

CONTINUOUS-TIME OPTIMIZATION OF GATE TIMING FOR SYNCHRONOUS RECTIFICATION

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Abstract

Synchronous rectifiers, which use a controlled MOSFET in place of a standard p-n or Schottky rectifier, are an important technology for low-voltage power converters. Conventional control techniques for synchronous rectification are often very conservative, however, leaving room for improvement. This paper presents a method for monitoring current flow to adaptively optimize the relative timing of two gate signals for a buck converter with synchronous rectification. Theoretical development is given, along with experimental results for two low-voltage converters.

1. INTRODUCTION

Since power MOSFETs became available in the mid-1980's, their use as synchronous rectifiers has been discussed [1]. The low on-state resistance $R_{ds(on)}$ of advanced MOSFETs motivates the added complexity. The result can be greatly increased efficiency, especially at very low output voltages.

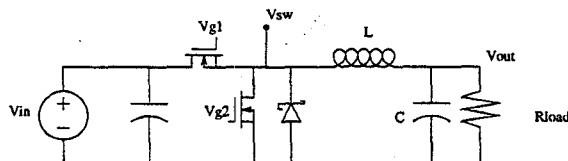


Figure 1: Synchronous Buck Converter

The disadvantage is an increase in support circuitry. Additional controls are necessary to prevent shoot-through, in which both devices conduct simultaneously. A typical approach is to introduce some dead-time, in which both gates are held low to ensure complete turn-off. This approach reduces the benefits of using the MOSFET, since some other device must carry the current during the off interval.

Many methods for synchronous rectifier control have been offered, each with their drawbacks. Older techniques, described in [1]-[3], use transformers with extra windings to drive the gates. In [4], combinational logic is used for direct emulation of a diode function. Unfortunately, this approach is limited by the speed of the comparators necessary for A/D conversion. A discrete-time adaptive algorithm is proposed in [5], which measures terminal voltages during one cycle to generate a gate signal for the next signal. As with many adaptive algorithms, the region of convergence for this algorithm is limited, and also relies on steady-state operation. None of these solutions greatly improves upon fixed dead-time circuits.

The algorithm presented here operates in continuous time to dynamically minimize the input current. Since efficiency is the ultimate goal and input voltage is considered fixed, minimal input current corresponds to maximum performance. Experiments have shown that three widely separated local minima exist: one where the synchronous rectifier never turns on, one where it never turns off, and one at the global minimum. Timing limits can exclude the first two, leaving only one. Results are given for two converters with 5 V inputs, one with 2 V output at 1 W, one with 1 V output at 10 W.

2. THEORETICAL DEVELOPMENT

Ultimately the goal of replacing a rectifier with a MOSFET synchronous rectifier is to reduce loss, which increases overall efficiency. Given fixed input and output voltages, the only degree of freedom is the relative timing of the gate signals in the converter MOSFETs. The power loss by both conduction and switching is a non-monotonic function of switch timing with a single minimum. A correlation-based control scheme can be used to maximize efficiency or, equivalently, minimize input power.

First, let us consider a general approach to correlation-based control. For continuous functions, this technique has been developed in [6]-[7], while a similar discrete-time

method is discussed in [8]. Here, the technique is extended to a combination of continuous and switching functions. The goal of the control technique is to maximize or minimize a given cost function J . The present discussion is restricted to minimization. Suppose there is some switching function x which affects J . Define x as follows:

$$tri(t) = 2 \left| 1 - \frac{2 \text{mod}(t, T)}{T} \right| - 1 \quad (1)$$

$$x(t) = \text{sgn}(d - tri(t))$$

making $tri(t)$ a triangle wave and $x(t)$ an asymmetrical square wave with duty ratio d . In a pulse-width modulation (PWM) system, the most appropriate control variable is d , because $tri(t)$ is relatively easy to generate and a comparator can generate $x(t)$ from $tri(t)$ and d . The implicit assumption is that d is always positive, but an equivalent definition can be made such that $d < 0 \Rightarrow x < 0$. In either case, d must be constrained to be non-zero.

Armed with these definitions, a nonlinear control law can be formulated as follows:

$$d(t) = -k \int_0^t x J dt = -k \int_0^t x \frac{\partial J}{\partial d} d dt \quad (2)$$

This is a correlation function between x and J . The actual implementation is of the first equality, while the second equality lends itself to further analysis. The gain k is somewhat arbitrary, but affects noise immunity and response time. Taking the derivative of both sides and combining terms gives

$$\dot{d} \left(1 + kx \frac{\partial J}{\partial d} \right) = 0 \quad (3)$$

Examination of either (2) or (3) can show that when $(\partial J/\partial d)$ is zero, implying J is minimized with respect to d , then d is no longer changing. Because d is constrained to be non-zero, there is no trivial solution. Further examination shows that when $(\partial J/\partial d)$ is negative, d is increasing, while when $(\partial J/\partial d)$ is positive, d is decreasing, consistent with approaching the minimum of $J(d)$. Simulation results for a hypothetical cost function $J = (d - 1)^2$ are shown in Figure 2, including noise in J . The simulations verify the foregoing discussion—essentially perfect steady-state behavior, with response time and noise immunity determined by the gain k .

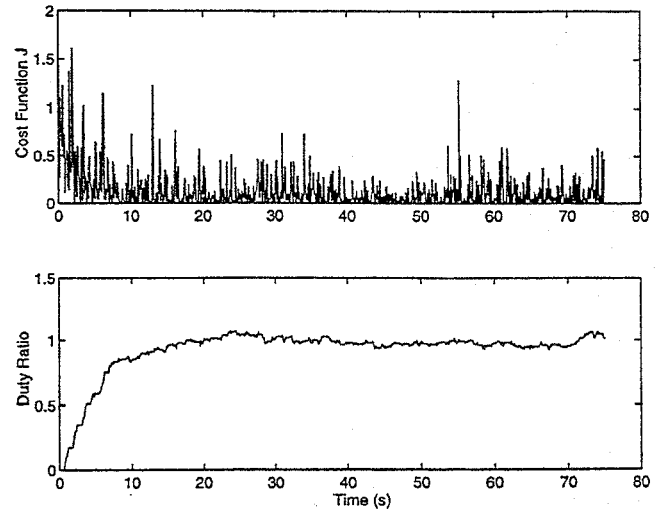


Figure 2: Theoretical Response

3. DEVELOPMENT OF TIMING CONTROL

Now consider applying the technique to the problem of gate signal timing for a synchronous rectifier. During the two transition times of each converter switching cycle, the inductor current i_L must commute from one device to the other. Choose the cost function J to be the input current I_m , to optimize efficiency. Alternatively, the choice could be $J = P_{in} = V_{in} I_m$, more accurately reflecting the desired goal. V_{in} is not subject to control, however, and an input capacitor should keep it essentially constant even during transients.

A quasi-static analysis gives a qualitative form for $J(d)$ by considering only conduction losses. Assume for simplicity that turn-on is immediate, while turn-off takes some amount of time. The main current being commutated is the inductor current i_L . When a MOSFET is on, the conduction loss can be approximated with a resistive drop R . For convenience, approximate the effective resistance of the diode to be the same as the on-resistance of a MOSFET. Let d' represent the time difference for actual conduction in the two MOSFETs. Then some circuit analysis shows:

$$P_{lost} = i_L^2 R + \frac{d'}{T} \left(V_d i_L u(d') + \frac{V_{in}^2}{R} u(-d') \right) \quad (4)$$

for a total conduction interval T , where $u(\bullet)$ is a unit step function. In actual operation, there is some time delay d_o between commanded turn-off and actual turn-off. Equation

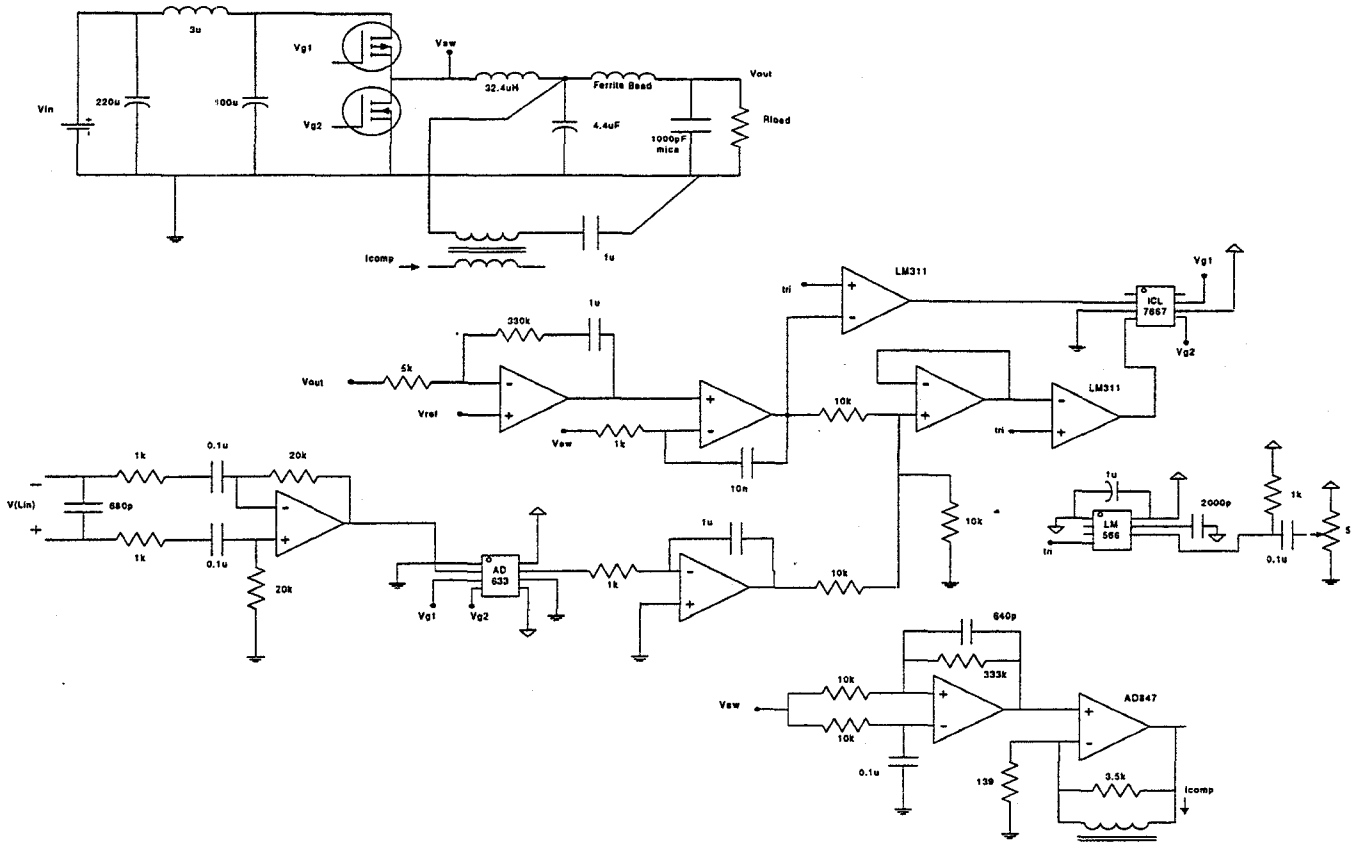


Figure 4: 5 V to 2 V, 1 W Synchronous Converter

(3) holds for measured signals if d' is replaced by $(d - d_o)$. For typical values of R , V_d , i_L , T , and d_o , Figure 3 shows P_{lost} as a function of d .

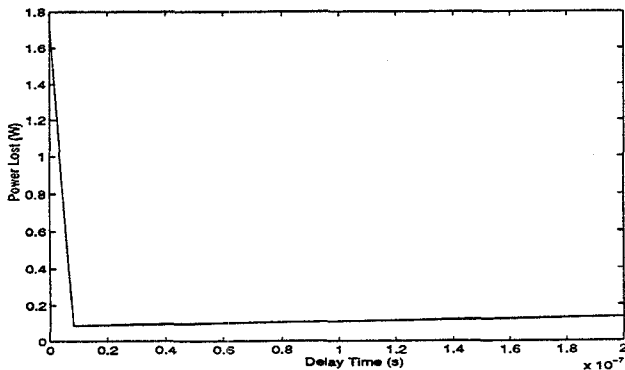


Figure 3: Theoretical Power Lost

Following the development in Section 2, the algorithm requires a square-wave function. Experiments show that the algorithm works effectively using a switching function instead: rather than alternating between +1 and -1, x alternates between +1 and 0. For power conversion, the gate signals V_{gs1} and V_{gs2} have to be generated as switching functions displaced by some d . Some combination of the two gate signals could be used to create $x(t)$. In the

original implementation for a 5 V input to 2 V output at 1 W, the high-side MOSFET is a P-channel device, which conducts when $V_{gs1} = (V_{g1} - 5)$ is negative. A switching function with duty ratio d can be generated by simply using the difference in gate voltage, $\Delta V_g = (V_{g2} - V_{g1})$, which can be easily measured with a single op-amp.

The algorithm requires information about input current. The standard method for current measurement involves a resistive shunt. In this case, a shunt is unacceptable because it adds loss. An alternative method involves an input inductor. Inductance at the input is useful for reducing current ripple at the source, if appropriate capacitance is included. The inductor provides a method for direct measurement of the time derivative of input current.

The final algorithm used in a converter with one P-channel device is

$$d(t) = -k \int_0^t (V_{g1} - V_{g2}) V_{L_{in}} dt \quad (5)$$

Implementation issues and results are discussed in the following section. The algorithm of Equation (5) conforms

to the general structure discussed in Section 2, and therefore should give consistent results regardless of device parameters or other factors which would affect $J(d)$.

4. IMPLEMENTATION AND RESULTS

The technique of (5) has been investigated in a 2 V, 1 W buck converter shown in Figure 4. Gate signal measurements are done as close as possible to the actual gate to reduce effects of trace resistance and lead inductance. Table 1 compares manual and automatic tuning. Manual tuning adjusted the dead-time to find the minimum input current for a given output. Clearly, the algorithm finds a point close to the optimum, but the flatness of $J(d)$ as indicated in Figure 2 limits the potential accuracy.

Table 1: Comparison of Manual and Automatic Tuning

Vout(V)	Pout (W)	η , manual (%)	η , automatic (%)
1.997	0.4373	80.90	79.86
1.996	0.6585	82.42	82.21
1.996	0.8680	82.39	82.20

Similar experiments were performed on a higher power converter, 1 V at up to 18 W. Results are shown in Figure 5. As losses increase at higher power levels, accuracy diminishes. One possible reason is that the high-side MOSFET had a much higher turn-off loss than expected, indicating that additional unmodelled loss processes are involved. This issue remains an area for future research.

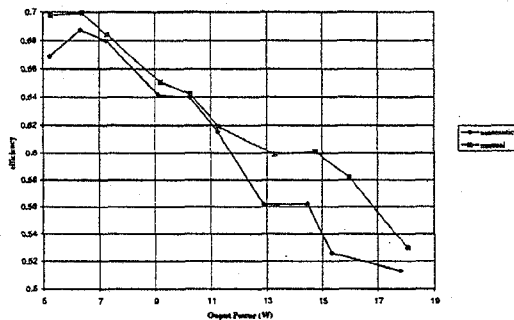


Figure 5: Efficiency of 5 V to 1 V, 18 W Converter

5. CONCLUSIONS

An effective method for adaptively optimizing gate timing for synchronous rectification has been developed. At low power levels, the method tracks optimum timing, and provides efficiency within 1% of the best possible value. There are no stability problems. This technique

exemplifies a new approach for synchronous rectifier controls, with many potential applications.

6. ACKNOWLEDGMENTS

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7. REFERENCES

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