

Digital SCR Control Box for Educational Laboratory

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Abstract— A “blue box” has been designed to introduce the silicon controlled rectifier (SCR) to power electronics students. SCRs are useful in many real-world applications, and are conceptually important in a student’s understanding of power converters. The box is highly flexible in application, and its internal design is simple enough to explain to students. Experiments are shown, both of the type commonly used in the laboratory and of the type used for demonstrations. The box has also been designed to be suitable for research purposes and line voltage applications.

I. INTRODUCTION

The silicon controlled rectifier (SCR) is an important device in the context of power electronics [1]. From a pedagogical point of view, it represents the natural evolution from diodes and uncontrolled rectifiers to controlled devices. It is typically one of the first power semiconductor devices introduced to students that allows direct control of power transfer. Typical converters implemented with SCRs have a great educational value. It is easy for students to understand their operation. SCRs also have the advantage that power circuits implemented with them are very forgiving, because natural commutation and turn-off primarily dictate circuit behavior (although dv/dt and di/dt issues cannot be ignored) [1]. Because of this, timing of gating signals is not as critical as with converters that use transistors or other forced commutation devices.

Student experience with converters is particularly important. Thus, it is necessary to provide test beds that allow implementation of circuits without the complexity of gate drive and timing circuit design. But it is equally important that students are well aware of some of the implementation details of the tools provided. With those premises in mind, a “blue box” design philosophy has been followed when designing test beds [2]-[4]. The main goals of the blue box approach are to facilitate converter experiments, design the test beds with typical and simple implementations of gate drives and timing circuits, and to expose the students to the actual implementation of the design tools.

Details about a FET box for an educational power electronics laboratory have been discussed in [4]. This paper covers the design and capabilities of the SCR box.

II. BACKGROUND

As part of the blue box philosophy, a simple conceptual design is required; therefore the SCR box implementation has no innovation in gate drive topology or timing concepts. The

basis for the design was previous generation SCR boxes [2]. The main idea was to overcome some of the limitations of those boxes and to provide additional capabilities that increase the number of applications that can be implemented with the SCR box. In the end, this extends the educational value of the boxes and even allows them to function as research grade test beds.

III. SCR BOX DESIGN

A block diagram of the SCR box implementation is shown in Fig. 1. The main idea is to generate a signal that follows the phase voltage associated to the phase A SCR to synchronize the timing required to fire the SCRs. Two input sources are provided, the power supply input voltage and an isolated external trigger input. This main trigger signal, a square wave representation of the ac input voltage, is fed to the phase A delay generator. Phase B and C delay generators are cascaded from the output of the phase A delay generator. Each delay generator is connected then to a gate pulse generator and a gate drive that ultimately drives the corresponding SCR. A master delay setting controls the phase A delay, while a phase-to-phase delay setting controls the phase B and C delays. The delay settings represent the number of pulses from the time base generator, which represent a particular delay. The time base is either a fixed clock (absolute timing) or the output of a PLL locked to the main trigger signal (angle based timing).

A digital design was followed, to simplify most of the implementation details, but more importantly to allow greater repeatability of results and to provide near calibration-free operation of the boxes. Full details about the SCR box design, including design documents, mechanical drawings

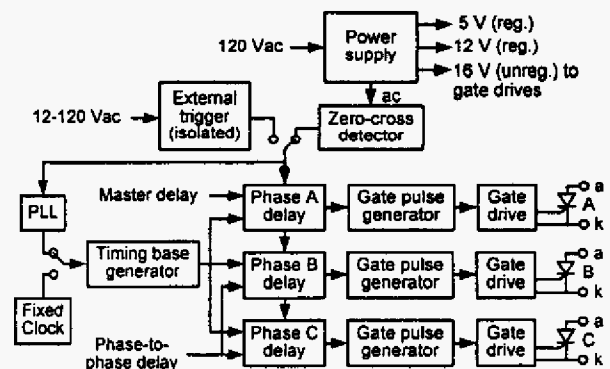


Figure 1. SCR box block diagram.

and schematics can be found in [5] and [6].

Because the boxes are meant primarily for student use, the user interface is of great importance. Fig. 2 shows a diagram of the front panel of the SCR box. The delays are specified by means of an optical encoder and two selection switches. A delay selector switch specifies the delay to be modified and a coarse/fine switch allows increments or decrements of 100 or 5 ms. Additionally, an analog source can be specified to control the master delay directly, by means of an A/D converter. To facilitate full-bridge operation of the boxes, a trigger inversion switch is provided, which allows the specification of a single master delay control α . For convenience, a trigger enable switch is also provided. The switch overrides the pulses presented to the gate drives, but otherwise leaves the whole timing sequence undisturbed. The back panel of the box contains the external trigger input and trigger selection switch.

The characteristics and capabilities of the design are summarized in Table 1.

Table 1. SCR box capabilities.

Digital control	Allows better repeatability of results and minimizes calibration requirements. Control is implemented in software in a microcontroller and a programmable logic device, therefore design changes are possible.
Delay readout	Eliminates guessing since displays the actual delay specified, as opposed to analog potentiometers. Can be calibrated to show number of pulses, time or angle representing each delay.
Internal trigger source	Useful when an outlet synchronized to phase A is available. Immunity to line voltage noise is excellent.
External trigger source	Useful when there is no relationship between the ac input powering the box and phase A. Allows the use of sources other than 60 Hz, and phase-to-phase voltages as a trigger source. Provides electrical isolation. Reduced noise immunity; filtering of the input voltage noise introduces delay.
Time base delay	Valuable for educational purposes, since requires students to convert delays in degrees to time. Useful when a fixed frequency voltage is used or when absolute timing is required.
Angle based delay	Useful with variable frequency sources. Allows direct control of the delay angle independently of frequency.
Analog master delay control	Useful to control several boxes at once. Allows the implementation of closed-loop systems.
Variable phase-to-phase delay	Critical for variable frequency applications. Allows control of one-, two- and three- phase circuits. Also has educational value, since it explicitly shows students the effect of an improper delay selection.
Trigger inversion	Facilitates implementation of full bridge converters from a single control α .
Calibration delay	Used to override delays introduced when using the external trigger. Also useful when there is an absolute phase difference between phase A and the ac input powering the box.
Number of phases	One-, two- and three-phase control can be implemented with a single box. Four-, five- and six-phase control possible with two boxes
Delay range	Can be made arbitrary by adjusting the time base clock. Allows two-quadrant converter operation.
Power handling	Input voltages up to 130 V _{rms} and output currents up to 10 A for a power handling capability of 650 W per phase. Tested up to 1.3 kW three-phase power, with a case temperature of 56 °C in a 22 °C ambient.

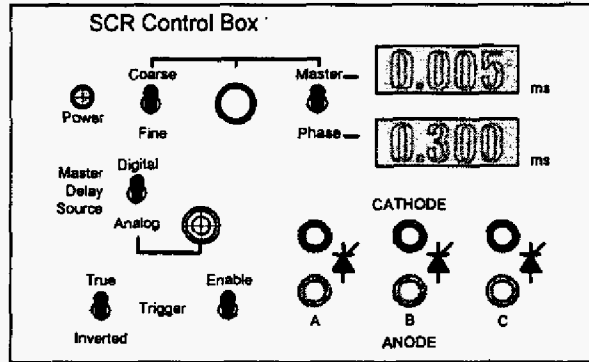


Figure 2. SCR box front panel diagram.

IV. EXPERIMENT EXAMPLES

To illustrate the capabilities and possible educational uses of the box, several experiments were implemented. Intended to be demonstrated in an educational laboratory, the experiments use low voltage. Experiments one and three can be easily integrated into a normal educational laboratory experiment, while experiment two is better suited for a demonstration due to the complexity of the setup. Additionally, a simple line-voltage experiment demonstrates the high voltage and high power capabilities of the design.

A. Full-bridge controlled rectifier

A three-phase full-bridge controlled rectifier [7] was implemented for a 25 V source. A diagram of the implemented circuit is shown in Fig. 3. The (dc) output voltage of the converter is given by

$$\begin{aligned} \langle v_{out} \rangle &= \frac{3V_0}{\pi} \sin\left(\frac{\pi}{3}\right) [\cos\alpha - \cos(\alpha + 180^\circ)] \\ &= \frac{6V_0}{\pi} \sin\left(\frac{\pi}{3}\right) \cos\alpha \end{aligned} \quad (1)$$

where α is the control delay angle and V_0 is the input voltage amplitude. Resistive, inductive and motor loads were tested. Fig. 4 shows typical waveforms for an unloaded motor load with extra external inductance. Ch1 is the phase A line current, Ch2 the motor current, Ch3 the motor terminal voltage and Ch4 is the converter output voltage. The machine used is a 1/9 HP, 24 V, 4200 RPM dc motor. The delay angle was adjusted for rated machine voltage. Because of the extra inductor, the machine's induced voltage can be

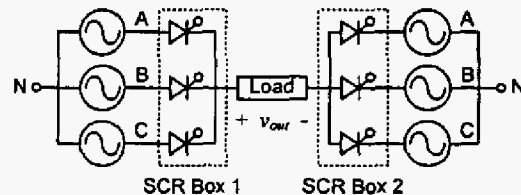


Figure 3. Three-phase full-bridge controlled rectifier.

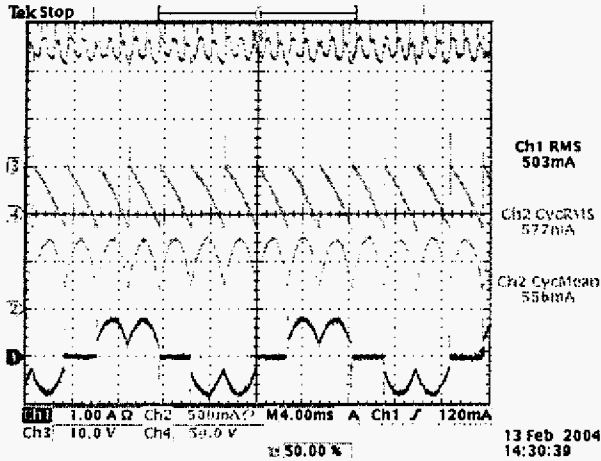


Figure 4. Full-bridge waveforms for a dc motor load.

monitored directly without requiring the armature current to go to zero.

B. Dc transmission line simulation

A dc transmission line can be implemented by using full-bridge rectifiers on both ends of the line [8], [9]. A 25 V simulation of a dc transmission line was implemented using 25 mH inductors to represent a long line, as shown in Fig. 5. Since the rectifiers are two-quadrant converters, power flow can be in either direction. Adjustments to the delay angles α and β control real and reactive power flow at the ends of the line.

Figures 6 and 7 show input and output phase A voltage and current corresponding to a 185 W transfer at 77 % efficiency for $\alpha = 30^\circ$ and $\beta = 154^\circ$ with a 4 A link dc current and a 50 V average link dc voltage. Input power factor is approximately 0.95 due mainly to harmonic distortion. Output power factor is approximately 0.6 with a significant displacement angle between fundamental voltage and current. The low efficiency is a result of I^2R losses in the inductors.

The converter efficiency for a wide range of operating conditions is shown in Fig. 8. Efficiency is shown as a function of the average link current and parameterized by the delay angle α . Each dc current level corresponds to a particular value of the delay angle β . The values of α smaller

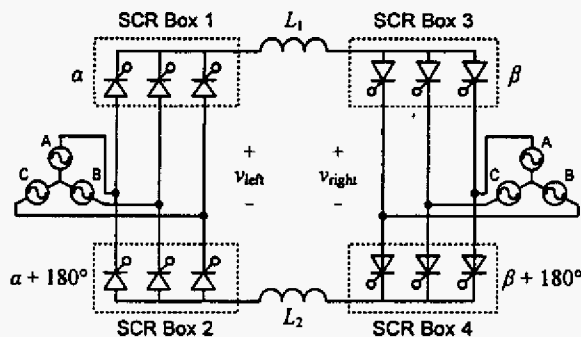


Figure 5. Dc transmission line diagram.

than 90° correspond to a left-to-right power transfer and the power flow is reversed for values of α larger than 90° .

C. Controlled battery charger

To demonstrate feedback control using the box, a simple 24 V battery charger was implemented, as shown in Fig. 9. The circuit uses battery voltage and current information to enforce a voltage limit and to track a reference charging current. The nonlinear control law implemented is

$$\alpha = \alpha_0 + k_1 e + k_2 \int e dt \quad \alpha_{\min} \leq \alpha \leq \alpha_{\max}$$

$$e = i_{bat} - i_{ref}$$

$$i_{ref} = k_0 v_{comp}$$

$$v_{comp} = \begin{cases} V_0 & v_{bat} < v_{ref} \\ 0 & v_{bat} \geq v_{ref} \end{cases} \quad (2)$$

where α_0 is a nominal delay angle, α_{\min} and α_{\max} are limits on the delay angle, V_0 is a reference voltage and k_0 , k_1 and k_2 are controller gains. Both v_{bat} and i_{bat} are low-pass filtered before

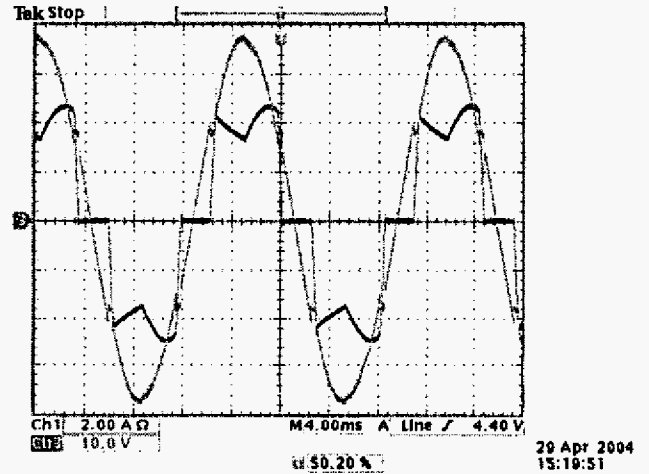


Figure 6. Dc transmission line phase A input voltage and current.

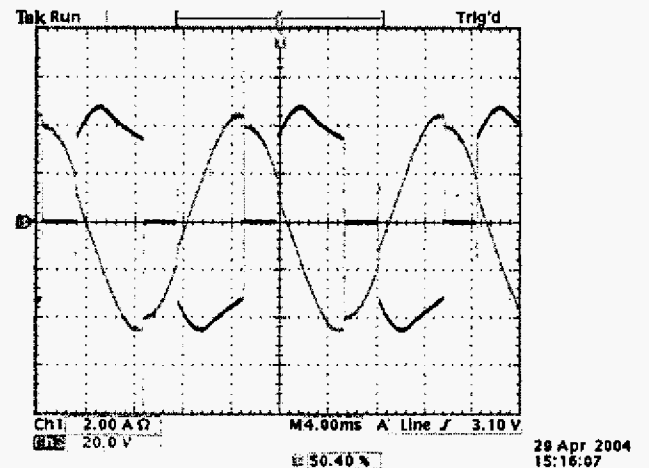


Figure 7. Dc transmission line phase A output voltage and current.

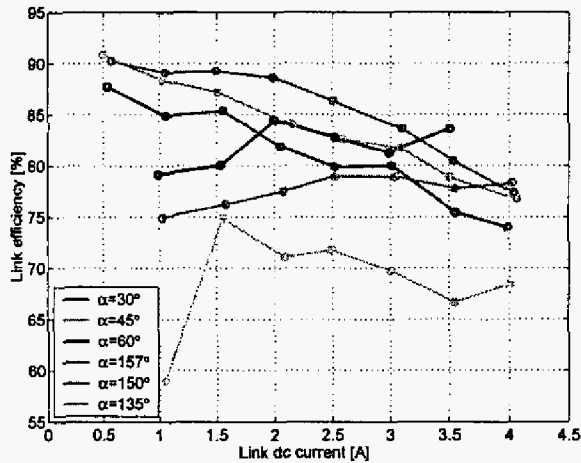


Figure 8. DC transmission line efficiency.

being used in the control law. This control law is easily implemented with three opamps, a comparator and passives.

Fig. 10 shows typical waveforms for the implemented circuit for a (average) charging current of approximately 100 mA. Ch1 is the battery current, Ch2 is the control signal, Ch3 is the battery voltage and Ch4 is the converter output voltage. The waveforms show the (average) charging current following its reference value and it can also be seen how once an over-voltage condition is detected, charging is stopped. Hysteresis ensures that charging will resume once the battery voltage dips sufficiently.

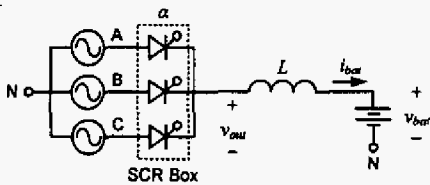


Figure 9. Half-bridge battery charger diagram.

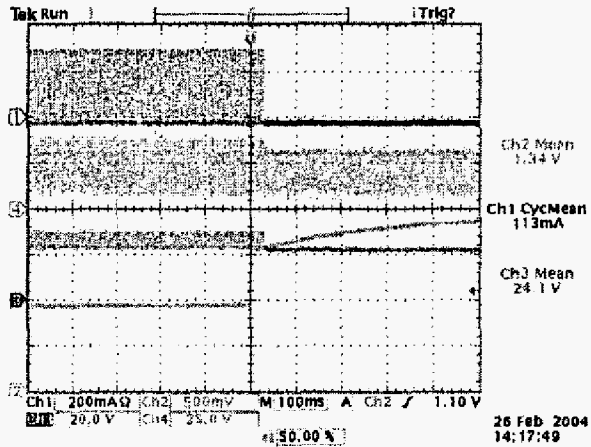


Figure 10. Battery charger voltage limit enforcement.

D. Line-voltage half-bridge controlled rectifier

To illustrate the high voltage and high power capabilities of the box, a 208 V (phase-to-phase) input, three-phase half-bridge controlled rectifier with a 13 Ω resistive load was implemented in the laboratory. The circuit diagram is the same as Fig. 9, but with the inductor and battery replaced by a resistor. Fig. 11 shows sample waveforms for a delay $\alpha = 90^\circ$. Ch1 is the output current, Ch2 the output voltage and Ch3 the phase A input voltage. Fig. 11 shows the output dc voltage and power as a function of delay, consistent with theoretical expressions for these quantities.

V. CONCLUSION

A digital SCR experimental design tool intended for an educational laboratory has been discussed. The capabilities of the box allow the implementation of a wide range of converters and experiments, including the use of feedback control. Flexibility of the design facilitates the development of both educational and research grade experiments. Line voltage operation of the box was demonstrated and confirms the high power processing capabilities of the design.

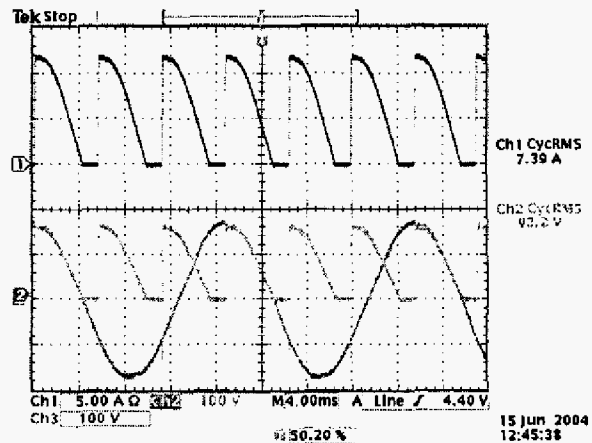


Figure 11. Line voltage rectifier waveforms for $\alpha = 90^\circ$.

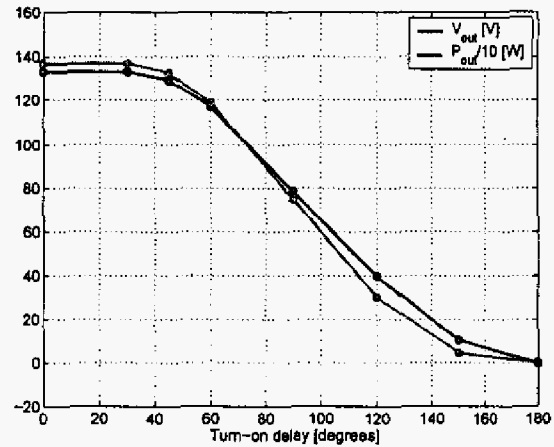


Figure 12. Line voltage rectifier output characteristics.

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