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DIGITAL CONTROL TECHNIQUES FOR SWITCHING POWER CONVERTERS

BY

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DISSERTATION

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ABSTRACT

Digital control methods for switching power converters offer greater robustness, more flexibility to changing operating characteristics, and better system performance than conventional techniques, which are often model-limited and only work well in a small range of conditions. Digital controllers are broadly classified into five generations, from 0 through 4. Generation 4 methods, such as the three techniques proposed in the present work, use new system formulations to achieve advanced control objectives. The first proposed technique is a singular perturbation analysis that provides a theoretical foundation for time-scale separation. If a buck, boost, buck-boost, or flyback converter meets a simple requirement, then inductor current operates on a fast time scale while the capacitor voltage changes on a slow time scale. This separation enables other control techniques. The second new technique employs a Kalman filter to create a sensorless power factor correction (PFC) controller. The proposed method uses voltage measurements in a switching power converter to eliminate the need for current sensing. An experimental converter that meets regulatory requirements validates the system. Finally, an online optimization method, discrete-time ripple correlation control (DRCC), is shown to automatically operate a switching power converter at an optimal point, such as maximum power from a source. DRCC is derived, stability is proven, and an application to a photovoltaic system is demonstrated experimentally. These three techniques together form a toolbox for future control applications.

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CHAPTER 1

INTRODUCTION

Digital control techniques enable switching power converters to meet the demands of new and growing applications. Advantages include better performance in the presence of noise and uncertainty, optimal system operation, and flexibility in changing conditions. While conventional analog methods are limited to particular structures, digital methods are theoretically unlimited. As hardware capabilities—sample rate, resolution, and computation speed—improve, so can controller performance.

The control of switching power converters is varied. For background purposes, conventional analog methods are described in Section 1.1. Then digital control “generations” are defined in Section 1.2 so as to form a simple taxonomy. Generation 1 controllers use digital elements in a supervisory role. Generation 2 controllers use z -transform methods. Generation 3 controllers use nonlinear methods in a deterministic, sampled-data framework. Generation 4 controllers start from a fundamental analysis of the system, including time-domain, stochastic, and ripple effects, to achieve new control goals.

The present work provides three new Generation 4 tools for digital control design. Time-scale phenomena are studied as a foundation. A stochastic framework is presented and used to design a control system with limited sensors. An online optimization technique that performs well with limited sample rates and computations is developed. With these three tools, broader adoption of digital control methods becomes possible.

1.1. Background and Definitions

Switching power converters are circuits that efficiently convert electrical energy from one form to another. They may be broadly classified according to their input and output forms: ac-ac, ac-dc, dc-ac, and dc-dc; or according to their function: power supply, motor control, lighting, etc. A typical switching power converter is composed of semiconductor switches, passive energy storage devices, and control circuitry. Example semiconductor switches are diodes, SCRs (silicon controlled rectifiers), BJTs (bipolar junction transistors), MOSFETs, and IGBTs (insulated gate bipolar transistors). Energy may be stored in inductors or capacitors; usually, capacitors serve a filtering role, while inductors fulfill the energy storage role. Some converter topologies include transformers or coupled inductors for isolation. The design of power circuits (switches and passives) has been the subject of extensive research [1]. A buck converter, which exemplifies many of the aspects of switching power converters, is shown in Fig. 1.1. The control circuitry can be analog, digital, or mixed-signal.

Control objectives vary according to the application and include output regulation, input regulation, and layered or nested objectives. A typical power supply requires only output voltage regulation. Some systems, such as battery chargers and lighting systems, require output current regulation. Combinations, where output current regulation is used

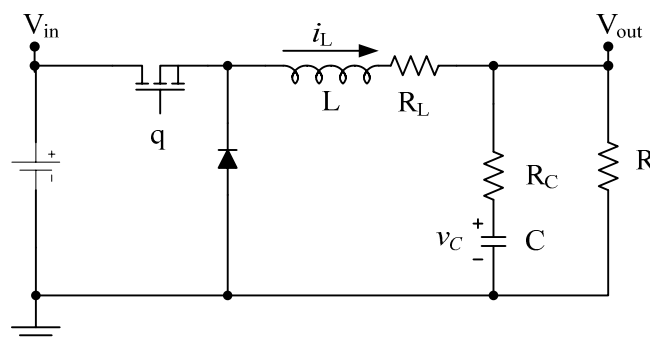


Fig. 1.1. Buck converter.

to supplement voltage regulation, enable improved performance or protection. Two examples of input regulation are power factor correction (PFC), which forces input current to track a reference waveform, and maximum power point tracking (MPPT), which adjusts input current and voltage to extract maximum power from a soft source. Systems with layered objectives include adjustable speed drives (ASDs), which are switching power converters that control induction motors. A typical ASD controls current, flux, torque, speed, and possibly position in a nested control structure. While simple voltage regulation can be achieved with an operational amplifier, an oscillator, and a comparator, an ASD usually requires an advanced digital controller.

To meet a particular control objective, any controlled switch may be turned on or off at any time. However, this formulation has too many degrees of freedom. Many modulation schemes have been proposed that forsake this freedom in exchange for simpler implementation. The most common technique is pulsewidth modulation (PWM), in which a controlled switch is turned on and off at a fixed frequency with variable duty cycle. This fixed frequency may be aligned with the centers of the pulses or with the rising or falling edges. Or, the frequency may be variable, as in random PWM. The development of alternative formulations that have different time-domain or frequency-domain behavior and that exploit other aspects of the general formulation is an active research area [2, 3].

Conventional power supply controllers are based on analog (or more properly, mixed-signal) ICs. A wide range of control ICs is available to implement voltage mode control, current mode control, and current regulation, usually with a PWM process. Most are designed for closed-loop operation, although many support open-loop operation as

well. A typical mixed-signal power supply controller includes an oscillator that sets the switching frequency, a comparator that compares a ramp and a reference to create a PWM signal, logic for protection modes, and a gate drive output to control a MOSFET, BJT, or IGBT. An operational amplifier and reference are almost always included to directly support a closed-loop system. Figure 1.2 shows a block diagram of a TL598, one of the simplest mixed-signal PWM ICs. More advanced ICs may have multiple feedback paths, additional operating modes (such as pulse frequency modulation), and even internal MOSFETs. Specialized ICs support lighting applications or PFC. Conventional power supply designs use off-the-shelf ICs for low cost and convenience.

Digital control methods offer many advantages over conventional analog techniques, such as reprogrammability, tolerance to component variation, support of multiple operating modes, better efficiency, and better performance. Their primary disadvantage is high cost. A digital controller comprises many technologies that are relatively new (and therefore more expensive than analog devices), such as an analog-to-digital converter (ADC) for feedback, a digital core for signal processing and loop closure, and a mechanism for creating switching signals. As semiconductor technology

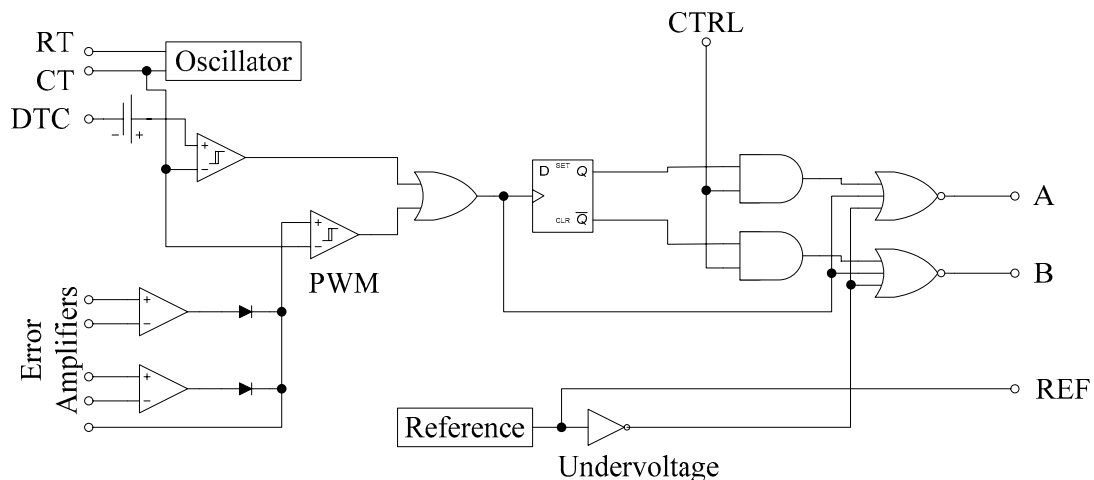


Fig. 1.2. TL598 block diagram (simplified).

matures, however, digital controller costs will continue to drop so that more systems can benefit from these advantages.

1.2. Digital Control Generations

Digital controllers can be divided into five generations that, rather than being a temporal sequence, reflect a progression in capabilities. A conventional analog system can be termed Generation 0, since it includes digital elements. A typical “analog” PWM block includes a comparator and a latch; other digital gates and latches are often included to support overvoltage, undervoltage, overcurrent, and softstart functions. The feedback portion, though, is analog and is designed with Laplace-domain techniques.

Generation 1 controllers retain all of the elements of a Generation 0 controller and add digital supervisory elements. For example, a digital interface may adjust the output voltage setpoint or provide status feedback. Oftentimes, this approach is referred to as *digital power management* (DPM), since the actual control elements are conventional analog/mixed-signal. DPM is well-established in information technology equipment—everything from laptop computers to high-end servers. Generation 1 approaches achieve a few of the benefits of a digital approach, such as reprogrammability and possibly multiple operating modes.

Generation 2 controllers replace actual control elements with digital devices but use a conventional design methodology. For example, instead of an operational amplifier (op amp) -based feedback circuit, a Generation 2 controller could use a microcontroller to sample voltage(s) and/or current(s) and compute the command signal. Its feedback law would essentially be a z -transform equivalent of the replaced analog circuit. The actuation (PWM signal generation) could be performed within the microcontroller or

with an external mixed-signal circuit. The primary advantage of Generation 2 is that the design methodologies are familiar to experienced power electronics designers. IC suppliers currently compete for new designs by offering easy-to-use configuration software. Generation 2 approaches enable much more flexibility than analog systems, yet they do not achieve all of the benefits of digital hardware.

Generation 3 controllers begin with a digital framework, and so achieve most of the benefits of digital implementation. Multiple time scales and advanced nonlinear controllers are possible. Laplace-domain design is gone; usually, z -transform-domain design is only a small part of the total design. A good example is an ASD, which samples output currents at a high rate, dc bus voltage at a lower rate, and position at an even lower rate. Multiple control loops generate speed, torque, flux, and current references that culminate in PWM outputs. Unconventional pulse generation methods, such as space-vector modulation and direct torque control, are possible. However, Generation 3 controllers are seldom used outside the motor control application space.

Generation 4 controllers use switch-level models and time-domain techniques to achieve greater robustness, faster dynamic response, improved tracking accuracy, and noise immunity. Where Generations 0 through 3 have limited design options, Generation 4 includes a broad class of approaches. The objective of the present work is to demonstrate three Generation 4 techniques.

1.3. Work Summary

In Chapter 2, existing control techniques are summarized. Digital control has been researched for decades. One can point to 1981 as a threshold year, in which sampled-data models of switching power converters were first published [4]. Only

recently, though, have researchers focused on power supplies (ac-dc or dc-dc), rather than inverters (dc-ac). The literature review in Chapter 2 captures both the older, foundational research and the newer, specific research.

Chapter 3 uses singular perturbation theory to establish a time-scale framework for future control development. Where previously researchers have asserted a separation between current and voltage dynamics [5, 6], the analysis in Chapter 3 rigorously establishes conditions for such a separation. The primary result derives a relationship between inductance, capacitance, and parasitic resistances that must be satisfied in order to separate voltage and current time scales. If this relationship exists, inductor current dynamics can be analyzed with the capacitor voltage treated as a constant. Otherwise, the system exhibits typical second-order behavior. Then the control must simultaneously consider voltage and current dynamics. Several different systems are studied: boost, buck, buck-boost, and flyback converters; with resistive or constant-power loads; in continuous- or discrete-time formulations. Time scale analysis is foundational for two further applications, Kalman filters and discrete-time ripple correlation control (DRCC).

A Kalman filter is a signal-processing block that extracts useful information in a noisy environment, such as a line-connected switching power converter. Chapter 4 explores Kalman filters in the context of switching power converters. A Kalman filter-based sensorless PFC scheme is proposed, where adequate information is obtained from voltages so that the expensive, noisy current sensor can be eliminated. This demonstrates a system formulation that differs substantially from a Generation 2 approach. The power converter satisfies the time-scale separation requirements of Chapter 3 so that current and voltage dynamics can be considered separately.

Chapter 5 discusses DRCC, a new online optimization method. This builds on continuous-time ripple correlation control (RCC) and shows that a discrete-time implementation is simpler and has many application advantages. DRCC has been applied to solar panel maximum power point tracking. Since DRCC is a digital technique, other digital methods, such as supervisory control with multiple operating modes, can be easily added. The combination of supervisory control and an inherently robust optimization technique achieves excellent large-scale behavior. A stability proof is offered. An experimental system validates the predicted performance.

Chapter 6 summarizes the primary contributions of this dissertation and indicates areas for future research. Although digital control of power converters has been studied for decades, widespread use is still hindered by misconceptions. I hope that both researchers and practitioners will see the value of Generation 4 digital approaches. Many practicing engineers focus on Generation 1 approaches as the easiest way to add the value of digital systems. Most research publications fall broadly into Generation 2, although Generation 3 approaches are also becoming common. As the costs associated with digital ICs continue to decline, analog approaches will increasingly appear to be old-fashioned and expensive. Generation 4 techniques have great potential to effect broad changes in design methodologies and system performance. The present objective is to provide a “toolbox” that future researchers can apply to a wide range of problems.

CHAPTER 2

LITERATURE REVIEW

Each power converter control system design has three facets: plant models, architecture, and application-specific attributes. The power converter plant must be modeled accurately, in a form that is amenable to feedback or feedforward control. The control architecture should be defined in an appropriate framework for digital control, given the sensors available and a particular control objective. Overall, the controller must consider the application and any particular aspects that can be exploited or that need to be addressed. This chapter summarizes prior work in these three aspects of control design.

2.1. System Models

Control design depends foremost on good plant models [7]. Although a switching power converter is inherently nonlinear and time-varying, the nonlinearities can be neglected in most applications, such that the system can be modeled as a switched piecewise-linear system. Various techniques have been proposed to remove the time variation inherent to switching, since most control methodologies assume a time-invariant plant. State-space averaging [8, 9] is a conventional technique that removes all time-varying behavior and creates a nonlinear, time-invariant model. It essentially uses matrix exponentials and discards all terms that are quadratic in the switching period (the “fast-switching” assumption) to find an equivalent system. Many applications further simplify the model by linearizing around an operating point. Other averaging techniques [10-17] can capture switching-frequency effects to determine if they are relevant to the problem at hand. These advanced models include both time-invariant components and

time-varying components, both of which are infinite series. The differences among these methods include problem formulation and basis functions. The Krylov-Bogoliubov-Mitropolsky (KBM) method [10, 11], which performs symbolic decomposition of a switched system using piecewise-polynomial basis functions, is used in Chapter 3 to include some switching effects. One advantage of the KBM formulation is that the basis functions are piecewise-polynomial. In many switching converters, piecewise-linear approximations are adequate, so only one or two terms in each series is required. Though more complex, the KBM model is more accurate than a conventional state-space average and still admits symbolic and numerical analysis.

Sampled-data models [4, 18-21] are commonly used for digital control. A typical sampled-data approach is to integrate the switched differential equation set over one PWM cycle to determine the state transition matrix. This model is then valid only at sample instants. The integration process involves a product of matrix exponentials, which can each be computed with a Taylor series. If all quadratic terms are discarded, sampled-data models closely match state-space averaged models. Because circuit parameters vary due to temperature changes and manufacturing tolerances, controllers need built-in robustness, so that inaccuracy from discarding the quadratic terms is often irrelevant. Another modeling technique with few applications hybridizes averaging and sampling, that is, it samples the averaged model [22, 23].

Modeling approaches are dependent on the application. A linearized, state-space-averaged model is appropriate for an analog controller [7]. The full (nonlinear) state-space-averaged model is appropriate for some geometric controllers [24, 25]. A KBM average, or other higher-order average, is most appropriate for analysis or for fast

simulation [10-12, 17]. Sampled-data and hybrid models are typically used for digital control design [4]. Most of the following control techniques are based on sampled-data models. Chapter 3 uses state-space averaging, KBM averaging, and sampled-data modeling. Chapter 4 uses state-space averaging and sampled-data modeling. Chapter 5 uses sampled-data modeling and KBM averaging concepts. The next section describes several control architectures, most of which use sampled-data modeling or state-space averaging.

2.2. Control Architectures

Control systems can either use full state knowledge or a reduced set of sensors. Full-state feedback control [26] requires both voltage sensing and current sensing. While voltages are easily measured, current sensing can be problematic. At high power levels, Hall-effect current sensors are commonly used [1]. Low-voltage and low-power converters typically cannot use them, though, because they are large and expensive. The typical sensor for low currents is a resistive shunt, which gives small, noisy signals [27, 28]. Several approaches have been proposed to eliminate the need for current sensing. Sensorless current mode (SCM) control [28-33] is a well-studied analog alternative to conventional voltage mode and current mode controls. SCM control uses the integral of the desired inductor voltage to produce a flux observer. For linear magnetic elements, flux is directly proportional to current. SCM control has the benefits of both voltage mode and current mode controls. It can also be adapted to unusual circuit topologies, such as an input-series-output-parallel multiphase converter [34, 35], and to the digital domain [36]. Other methods that use flux estimates include one-cycle control [37] and an older method that requires an auxiliary winding on the main inductor [38, 39]. Discrete-

time current observers have also been proposed [40-42]. Lossless current sensing [6, 27] uses inductor voltage to estimate current. However, instead of observing the current dynamics, lossless current sensing uses the dc resistance of the inductor as if it were a sensing shunt. This limits the bandwidth of the larger control system. The adaptation of these sensorless methods to the digital domain is an active research area [36].

Predictive current control [43-49], though sensor-based, is related to SCM control and one-cycle control. In predictive current control, present current, future desired current, and known system voltages are used to determine the correct duty cycle to arrive at the target. The earliest method [46] was intended for motor control applications, which are primarily three-phase and usually need some estimation of motor back EMF (electromotive force). The approach in [44] uses an analog circuit to accomplish many of the objectives of the other techniques. The algorithm in [45] should be considered the prototype for future developments, as it is the most complete. Three variants are shown, which can control the peak, valley, or average current. Stability and robustness are addressed. The method in [43] is similar but with a different modulation process—where other methods use a PWM variant, this variable-frequency method uses constant on-time, variable off-time. All of these methods [43, 45-49] should be classified as Generation 3, as they deviate from standard z -transform design in a substantial way, yet do not fully consider all system dynamics.

If a designer chooses to use an observer instead of direct measurements, there are three basic approaches. Discrete-time deterministic observers [50, 51] are closely related to continuous-time observers, although there are some differences that result from timing delays. The observer-based method in [42] is similar to both predictive current control

and SCM. A second approach is to use system identification methods based on an injected disturbance [52]. System identification is generally more useful for parameter extraction (a supervisory control function) than for feedback control. The third approach is to use a Kalman filter [53, 54]. Kalman filters are developed from stochastic assumptions, that is, all state dynamics and measurements include additive Gaussian noise. This approach is inherently more flexible and will be discussed in detail in Chapter 4. Kalman filters are largely used as signal processing elements. Depending on the system formulation, Kalman filters can either be used inside the control loop, as a standard observer, or outside the control loop, as a system identification method.

Generation 2 approaches use conventional design techniques in the Laplace domain, and then convert the controller to the z -transform domain [26, 55-63]. The approach in [56] is representative; essentially, the controller operates in a linear (z -transform) mode most of the time. However, when a large state excursion is detected, a finite state machine allows the controller to deviate. Another approach, such as in [58], uses a conventional analog design methodology and allows the designer to automate the loop-closure process. Other approaches, such as [64, 65], use digital communication techniques to support flexible, modular power architectures.

A modest improvement, still classified as Generation 2, is to use gain-scheduling [61, 66, 67], in which several (usually linear) controllers are designed for multiple operating regions. As the states evolve, the supervisory control [68, 69] switches among the various controllers. While the underlying controllers are still designed with conventional methods, the overall control system takes advantage of digital capabilities to improve performance over a wider operating range.

Adaptive control [70], in which a supervisory controller dynamically adjusts control parameters, is a broader Generation 3 approach. Many examples are extant in the research literature. In [71], a disturbance is injected at multiple discrete frequencies to find system impedance, then an automated procedure determines feedback gains from impedance. In [72], an error detector automatically changes the sample rate to switch between 50-Hz and 60-Hz operation. In [73], capacitor voltage ripple is used to estimate capacitance, which then determines controller gain to maintain high performance. System identification methods intended for off-line analysis [74] can also be applied directly on-line for continual parameter updates [58]. The methods of [58, 74, 75] all use some external perturbation that contains many frequency components (effectively white noise) to extract parameter information. The methods of [41, 75, 76] apply auto-regression and related methods to various power converters. As adaptive control is an active research field, other applications to switching power conversion can be expected. These methods are particularly suitable when the system has structured uncertainty, that is, the converter structure is well-known and parameters vary within a limited range.

A number of Generation 4 digital control techniques have been proposed, many of which are specific to a particular application. In [77], an alternative control formulation seeks approximate output tracking, rather than exact output tracking. The proposed approach is more robust in the presence of unstable zeros. Digital control can be used to automatically tune a resonant converter [78]. Fuzzy logic has been applied to motor control drives [79-82]. Recently, fuzzy logic controllers have been proposed to handle unstructured uncertainty in dc-dc converters [83]. A more moderate approach is to retain a deterministic, model-based methodology and apply hybrid control concepts [2, 84].

Extremely fast disturbance response is possible [35, 85-87] through the study of fundamental switched system dynamics. This approach, though a major component of Generation 4 digital control, is beyond the scope of the present work. These and other Generation 4 techniques often require new modeling methods and are primarily applicable to a specific control objective.

2.3. Applications

Almost all ASDs use Generation 3 digital control to implement nonlinear motor control algorithms [88]. A typical ASD is composed of several large, expensive diodes, a large capacitor, and several large, expensive IGBTs, plus a control system. The expense of the power circuit usually dwarfs the controller cost, so the incremental cost of a digital controller is negligible. Also, the benefits of digital control are substantial.

Digital control is particularly appropriate for ASDs because of the need for high-quality sinusoids with low harmonic content, usually generated with uniformly sampled sine-triangle PWM (UPWM) [89-91] or space vector modulation (SVM) [92]. The sampling process injects harmonics both near the switching frequency and near the modulation frequency. Various methods have been proposed to improve the harmonic spectrum [93, 94]. An early digital technique was programmed PWM, usually in the form of harmonic elimination [3, 95-99], in which a switching pattern is chosen to obtain a specific harmonic spectrum. As shown in [3], the problem can be generalized and an infinite solution space exists. Particular solutions have different harmonics in the uncontrolled region. More recently, researchers have developed improvements to the typical UPWM to more closely approximate naturally sampled PWM (NPWM). In [100, 101], extrapolation and noise-shaping methods were applied to class D audio amplifiers.

In [102, 103], similar results were achieved, though with different terminology. Both approaches use a low-fidelity PWM process with an auxiliary loop that increases fidelity over multiple switching cycles. While standard UPWM remains the most common solution, many other digital approaches can create higher quality sinusoidal or audio output.

Other modulation schemes, such as delta modulation, Σ - Δ modulation, or synergetic control, are possible. Delta modulation [104-108], a simple method adopted from the signal-processing world, is similar to a one-bit PWM process: in each cycle, the switch is either on or off for the full cycle. The position of some state (or state vector) is compared to a threshold (or surface) at uniformly-spaced times to determine whether the switch should be turned on or off. Over many cycles, the average control goal is obtained. A more complicated multibit Σ - Δ process [100-102] achieves similar goals with much better waveform fidelity. Delta and Σ - Δ modulation can act either on a scalar (such as a current reference) or on the position of the operating point relative to a surface, so they are types of boundary control [24, 109]—usually, “delta modulation” applies to a one-dimensional system while “boundary control” applies to a system with two or more dimensions. In boundary control, the objective of the switching pattern is to force the states to stay on or near a surface in the state space. Synergetic control [24, 25] uses a PWM-like process to force state trajectories to lie parallel to the control surface. Hysteresis control, a common analog geometric technique, is uncommon in the digital domain because of the inherent frequency variation.

An active filter, which resembles an inverter, actively eliminates harmonics in an ac system [40, 71, 110]. In [110], the objective is to create a pure sinusoid regardless of

load. This controller makes special considerations for nonlinear loads, such as rectifiers (ac-dc converters) that draw current in pulses. The method, though posed as an uninterruptible power supply (UPS), could be used as a series active filter. The filter in [71] uses an FFT and an inverse FFT to explicitly control various harmonics in the line current. The three-phase active rectifier in [40] is designed to draw unity-power-factor sinusoidal current without current sensors. These and related methods have been proposed to act as series or shunt power filters, mostly in three-phase systems.

PFC, also referred to as active rectification or PWM ac-dc conversion [111-114], allows a single-phase ac-dc converter to draw sinusoidal current, just as an active filter ensures sinusoidal three-phase currents. In PFC, the objective is to convert single-phase ac power to dc power with near-unity power factor and near-zero total harmonic distortion (THD). Most PFC controllers are implemented with analog circuits [115-119]. Some analog techniques, such as [115], exploit discontinuous conduction mode. More conventional techniques use multiple control loops for current and voltage [116, 118, 119]. Digital methods have also been researched extensively [46, 48, 72, 120-125]. Digital PFC techniques generally fall into either Generation 2 or Generation 3. For example, [120] proposes a fairly conventional controller (Generation 2) with an advanced digital implementation on a field-programmable gate array (FPGA). By contrast, [48] proposes a Generation 3 system that uses an advanced current controller whose error is used in a voltage estimator. In [72], a hybrid is proposed—a basic controller that is conventional (Generation 2), coupled with a supervisory self-tuning filter (Generation 3). One of the most promising techniques for commercial applications is presented in [73, 123]. Here, multiple control loops are used with different sample rates. Most

importantly, a change of coordinates is used to generate a linear system from the nonlinear dynamics. Chapter 4 uses the change of coordinates from [73, 123] and a Kalman filter to provide a robust, sensorless PFC control scheme.

While PFC targets zero harmonics for one load, other related applications have been discussed. Optimized nonunity PFC [126, 127] exploits the freedom in the relevant regulations [128] to trade increased harmonic content for reduced component sizes. A modified PFC converter can act partially as an active filter to reduce system harmonics [129]. A grid-connected inverter can be created from a PFC-like stage and thyristors for commutation [130].

Optimization methods are frequently proposed, since the goal of power electronics is the efficient conversion of energy from one electrical form to another. For example, a photovoltaic cell has a well-defined optimal operating point where it delivers maximum power [131], which can be tracked with an MPPT [132, 133]. A particularly useful MPPT method, ripple correlation control (RCC) [30, 134, 135], is a subject of Chapter 5. RCC is a general-purpose optimal control technique that is particularly appropriate for switching power converters. The first published application of RCC was in a solar MPPT [136-142]. Photovoltaic systems often use digital control for enhanced system performance [143].

A more significant application of RCC is motor efficiency maximization [144-149]. Electric motors consume about 2/3 of all electrical energy produced worldwide [150]; induction motors consume more than half of this total. When an induction motor runs below rated load, maximum efficiency would be achieved at reduced flux. However, standard motor operation keeps the flux level constant. Besides RCC, many motor

efficiency maximization techniques have been proposed [80, 82, 151-166] that adjust flux based on the operating point.

Other optimization opportunities exist. RCC has also been studied for dead-time optimization [167, 168] and filter tuning [169]. Fast, optimal disturbance rejection is tractable in the digital domain [2, 36, 170-176]. Certain dc-dc converter applications call for efficiency maximization [177, 178].

Digital control is a flexible and powerful alternative to analog control. While the past few decades have seen its use in high-power, high-value applications, further developments in digital ICs and control methods will lead to widespread application to lower power conversion, particularly in specialized applications like PFC and photovoltaic interface. The following chapters introduce several tools that future designers may apply to advanced power conversion requirements.

CHAPTER 3

TIME-SCALE PHENOMENA

The study of time scales, important for any dynamical system, is critical for digitally controlled systems. Designers must understand relevant time scales when choosing sample rates and actuation rates. This chapter addresses possible time-scale separation between inductor current dynamics and capacitor voltage dynamics in two-state converters [179]. Engineering intuition is replaced with a formal condition. Experimental results on a boost converter and a flyback converter show that there are three possible scenarios: coupled dynamics; decoupled dynamics that are fast, with low efficiency; or decoupled dynamics that are slow, with high efficiency.

3.1 Background and Motivation

Conventional wisdom in power electronics is that inductor currents are “fast” while capacitor voltages are “slow.” The present objective is to analyze switching power converter dynamics rigorously to determine what conditions must be satisfied in order for the time scales to separate.

While time-scale separation is important for many dc-dc converters, PFC converters *require* separation for proper operation. The objective of a PFC converter is to force an inductor current to follow the input voltage waveshape (a rectified sinusoid), while the output capacitor voltage is as close to dc as possible. The typical solution is to use a large output capacitor to smooth out the power fluctuations from the input. The conclusion of the analysis to follow is that a sufficiently large capacitor will indeed create time-scale separation.

Singular perturbation theory [180] is a rigorous analysis technique for nonlinear systems that partitions a dynamical system into fast and slow subsystems. Section 3.2 will explain singular perturbations in the present context. Section 3.3 will start with a switched linear model of a boost converter, apply averaging theory to yield a nonlinear time-invariant model, and use singular perturbation theory to explore the dynamics. An experimental converter validates the theoretical results. Section 3.4 will show similar requirements and results for other converter types. Section 3.5 will analyze a sampled-data model. Section 3.6 will examine stability of interconnected systems. Section 3.7 will summarize and identify areas for future research.

3.2. Singular Perturbation Theory

A singularly perturbed system is a nonlinear time-invariant system whose states can be partitioned into slow variables \mathbf{x} and fast variables \mathbf{z} . The separation in time scales is determined by a small scalar ε . The system must be in standard form, where all variables and coefficients are normalized, to apply this method. The standard form for an autonomous system is

$$\begin{aligned}\dot{\mathbf{x}} &= \mathbf{f}(\mathbf{x}, \mathbf{z}, \varepsilon) \\ \varepsilon \dot{\mathbf{z}} &= \mathbf{g}(\mathbf{x}, \mathbf{z}, \varepsilon)\end{aligned}\tag{3.1}$$

The functions \mathbf{f} and \mathbf{g} may be nonlinear. Switching power converters also include a control input \mathbf{u} and disturbance input \mathbf{w} . The results to follow hold so long as \mathbf{u} and \mathbf{w} are exogenous (they do not depend on \mathbf{x} or \mathbf{z}). The extended standard form is

$$\begin{aligned}\dot{\mathbf{x}} &= \mathbf{f}(\mathbf{x}, \mathbf{z}, \mathbf{u}, \mathbf{w}, \varepsilon) \\ \varepsilon \dot{\mathbf{z}} &= \mathbf{g}(\mathbf{x}, \mathbf{z}, \mathbf{u}, \mathbf{w}, \varepsilon)\end{aligned}\tag{3.2}$$

For $\varepsilon \ll 1$, the dynamics can be separated into two time scales. On the fast time scale, \mathbf{x} can be treated as constant while the dynamics of \mathbf{z} are analyzed. On the slow time scale, \mathbf{z} can be treated as algebraic, rather than dynamic, while the dynamics of \mathbf{x} are analyzed. The fast variable \mathbf{z} can be approximated by

$$\mathbf{z} = \boldsymbol{\varphi}_0(\mathbf{x}, \mathbf{u}, \mathbf{w}) + \varepsilon \boldsymbol{\varphi}_1(\mathbf{x}, \mathbf{u}, \mathbf{w}) + \boldsymbol{\eta} \quad (3.3)$$

The algebraic functions $\boldsymbol{\varphi}_0$ and $\boldsymbol{\varphi}_1$ form an integral manifold. Most of the analysis of \mathbf{x} dynamics can use $\mathbf{z} = \boldsymbol{\varphi}_0 + \varepsilon \boldsymbol{\varphi}_1$. The dynamic variable $\boldsymbol{\eta}$ captures the off-manifold dynamics. That is, \mathbf{z} does not necessarily start on the integral manifold, so the dynamics of $\boldsymbol{\eta}$ capture the dynamic transition from an arbitrary point in the state space to a point on the manifold.

The following sections will find time-scale separation criteria for two-state converters: boost, buck, buck-boost, and flyback. In these cases, there are two states total. The partitioned subsystems, then, are each scalar. The control input is related to the switching function. The disturbance input is the converter input voltage. Initially, the load will be treated as a constant resistance. Later, a Norton equivalent load will be considered to generalize the analysis to constant-power loads.

3.3. Boost Converter Analysis

3.3.1. Switched linear model

The open-loop boost converter shown in Fig. 3.1 can be modeled as a switched linear system. A closed-loop version could be considered nonlinear and time-varying. The PFC application implies large variation in input voltage and inductor current; otherwise, the dynamics are identical to any other boost converter. The switched linear model is

$$\begin{aligned}\frac{dv_C}{dt} &= -\frac{1}{C(R+R_C)}v_C + h_2 \frac{R}{C(R+R_C)}i_L \\ \frac{di_L}{dt} &= -h_2 \frac{R}{L(R+R_C)}v_C - \frac{R_L + h_2(R\parallel R_C)}{L}i_L + \frac{v_{in}}{L}\end{aligned}\quad (3.4)$$

Here, h_2 is the switching function of the diode. All variables and coefficients must be normalized to put the system into standard form. The nominal output voltage is V_0 , the nominal output current is $I_0 = V_0/R$, and the switching period is T . With these definitions, the other variables can be normalized,

$$\begin{aligned}\hat{v}_C &= \frac{v_C}{V_0} \\ \hat{i}_L &= \frac{i_L}{I_0} = \frac{i_L R}{V_0} \\ w &= \frac{v_{in}}{V_0} \\ u &= 1 - d = \langle h_2 \rangle\end{aligned}\quad (3.5)$$

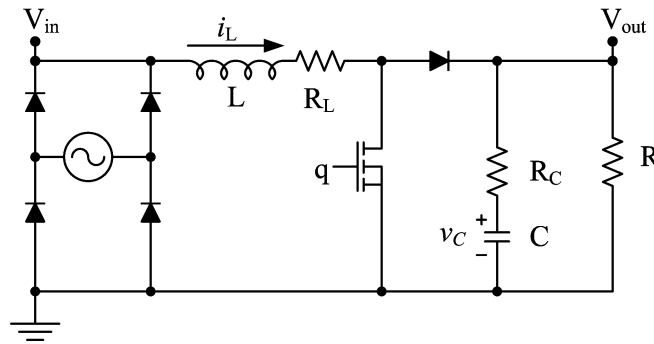


Fig. 3.1. Boost PFC converter.

$$\begin{aligned}
\hat{t} &= \frac{t}{C(R+R_C)} \\
p &= \frac{T}{C(R+R_C)} \\
\delta_0 &= \frac{R_L}{R} \frac{R+R_C}{R} \\
\varepsilon &= \frac{L}{R^2 C}
\end{aligned} \tag{3.6}$$

The normalized dynamical system is

$$\frac{d}{d\hat{t}} \begin{bmatrix} \hat{v}_C \\ \hat{i}_L \end{bmatrix} = \begin{bmatrix} -1 & h_2 \\ -\frac{h_2}{\varepsilon} & -\frac{\delta_0 + h_2 \frac{R_C}{R}}{\varepsilon} \end{bmatrix} \begin{bmatrix} \hat{v}_C \\ \hat{i}_L \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{R_C + R}{\varepsilon R} \end{bmatrix} w \tag{3.7}$$

3.3.2. Averaged system

Averaging can be applied to (3.7) to enable further analysis. Singular perturbation theory is only applicable to time-invariant systems. Since h_2 is a switching function, the model (3.7) is linear in the states and time-varying. State-space averaging [7-9], which removes all knowledge of switching frequency, is typically used to form a time-invariant converter model. Other methods retain switching information in time-invariant models. In particular, KBM averaging [10-12] is a simple algorithm that partitions a periodically varying system

$$\dot{\xi} = \alpha \mathbf{F}(t, \xi) \tag{3.8}$$

into a time-varying algebraic relationship

$$\xi(t) = \mathbf{y}(t) + \alpha \Psi_1(t, \mathbf{y}) + \alpha^2 \Psi_2(t, \mathbf{y}) + \dots \tag{3.9}$$

and a time-invariant dynamical system

$$\dot{\mathbf{y}} = \alpha \mathbf{G}_1(\mathbf{y}) + \alpha^2 \mathbf{G}_2(\mathbf{y}) + \alpha^3 \mathbf{G}_3(\mathbf{y}) + \dots \tag{3.10}$$

The new state vector \mathbf{y} corresponds to a moving average of the original states $\boldsymbol{\xi}$, while the algebraic series in $\boldsymbol{\Psi}$ models the ripple. The series in \mathbf{G} is time-invariant and admits further analysis. KBM averaging differs from generalized state space averaging [13] primarily in the choice of basis functions. While generalized state space averaging uses a Fourier approach (sinusoidal bases), the present KBM approach uses piecewise polynomials. Since most useful signals in a switching power converter are piecewise exponential, one would expect a summation of piecewise polynomial functions to fit the real signals with fewer terms than a summation of sinusoids. Terms past $\boldsymbol{\Psi}_3$ are usually negligible.

The switched linear system (3.7) fits the basic form of (3.8), so KBM averaging applies. Mathematica was used to find \mathbf{G} and $\boldsymbol{\Psi}$ terms (see Appendix C). For a boost converter, \mathbf{G}_1 is the conventional state-space average and \mathbf{G}_2 is identically zero. \mathbf{G}_3 is $O\left(\left(\frac{p}{\varepsilon}\right)^2\right)$ and captures the piecewise linear ripple in the states at the switching frequency. For a reasonable switching frequency, higher-order terms diminish rapidly. The complete averaged form through \mathbf{G}_3 is

$$\begin{aligned} \frac{dy_1}{dt} &= uy_2 - y_1 - \frac{1}{12} \left(\frac{u(1-u)p}{\varepsilon} \right)^2 \left(y_1 (\delta_0 - \varepsilon) + \frac{R_c}{R} \frac{R+R_c}{R} w \right) \\ \varepsilon \frac{dy_2}{dt} &= \frac{R+R_c}{R} w - uy_1 - \left(\delta_0 + \frac{R_c}{R} u \right) y_2 \\ &\quad + \frac{1}{12} \left(\frac{u(1-u)p}{\varepsilon} \right)^2 \left(y_1 \frac{R_c}{R} (\delta_0 - \varepsilon) + y_2 \varepsilon (\delta_0 - \varepsilon) + \frac{R_c + R}{R} w \left(\frac{R_c^2}{R^2} - \varepsilon \right) \right) \end{aligned} \quad (3.11)$$

A simple two-step analysis of (3.11) will establish time-scale separation criteria. First, the state-space-averaged system (using only \mathbf{G}_1) will be analyzed symbolically to

find a simple, verifiable relationship that determines whether or not time scales separate in a given converter. Then, results from an experimental converter will verify the conclusions. Finally, the actual parameters of the experimental converter will be substituted into (3.11) numerically to show that \mathbf{G}_3 has a minor effect on time scale phenomena since it is small for a continuous conduction mode converter.

3.3.3. Singular perturbation analysis

To put the averaged model (3.11) into standard form (3.2), we identify $x = y_1$ and $z = y_2$ and neglect all terms except \mathbf{G}_1 .

$$\begin{aligned} \frac{dx}{d\hat{t}} &= uz - x \\ \varepsilon \frac{dz}{d\hat{t}} &= \frac{R + R_C}{R} w - ux - \left(\delta_0 + \frac{R_C}{R} u \right) z \end{aligned} \quad (3.12)$$

All coefficients on the right-hand side must be normalized for singular perturbation analysis. Typically, $R_C \ll R$, so the coefficient of w in the second equation is slightly larger than 1. The coefficient of z , though, is typically small for a highly efficient converter. Define this coefficient to be

$$\delta(u) = \delta_0 + \frac{R_C}{R} u \quad (3.13)$$

The effect of this small coefficient $\delta(u)$ can be determined from an analysis of the approximate model (3.3). The complete approximate model includes both the algebraic terms (φ_0 and φ_1) and the η dynamical equation.

$$\varphi_0 = \frac{w \left(1 + \frac{R_C}{R} \right) - ux}{\delta(u)} \quad (3.14)$$

$$\varphi_1 = \frac{u^2 w \left(1 + \frac{R_C}{R}\right) - u^3 x - ux\delta(u)}{\delta^3(u)} \quad (3.15)$$

$$\varepsilon \frac{d\eta}{dt} = \left(\frac{\varepsilon u^2}{\delta(u)} - \delta(u) \right) \eta \quad (3.16)$$

The basic concept of a singularly perturbed system is that the fast dynamics decay, so that the relationship between x and z is dominantly algebraic. This requires η to have a stable equilibrium near the origin. A nonzero equilibrium is acceptable, but unstable dynamics are not. Stability of (3.16) requires the coefficient of η to be negative.

Algebraic manipulation gives a simple stability requirement:

$$\varepsilon u^2 < \delta^2(u) \quad (3.17)$$

If the converter parameters satisfy (3.17) at a given operating point, then there exists a separation between the dynamics of x and z or, equivalently, between v_C and i_L . The requirement is a function of the exogenous input u , while a designer would prefer a universally applicable requirement. To generalize, a stricter requirement can be found that does not include u , given that $u \in [0,1]$:

$$\varepsilon < \delta_0^2 \quad (3.18)$$

Both ε and δ_0 include the load resistance R in their definitions. Again, a stricter requirement can be found that does not include R ,

$$\sqrt{\frac{L}{C}} < R_L \quad (3.19)$$

Intuitively, Eq. (3.19) implies that the equivalent series LRC circuit formed by the inductor, its parasitic resistance, and the output capacitor must be overdamped. The key contribution of the present work is a rigorous derivation of the time-scale separation

requirement from basic circuit theory, nonlinear system theory, and singular perturbation theory.

3.3.4. Experimental verification

To demonstrate the relevance of (3.19), a simple boost converter was constructed. Parameters are listed in Table 3.1, with MOSFET resistance lumped into R_L . The design specification is for 12 V to 36 V conversion at 13 W. As constructed, this converter does not meet the requirement for time-scale separation. The characteristic impedance is

$$\sqrt{L/C} = 2.92 \Omega, \text{ which exceeds } R_L \text{ by about a factor of 5.}$$

With the basic converter that fails the separation criteria, a duty cycle step was applied, from 67% to 64%. Inductor current and output voltage are shown in Fig. 3.2. Classic second-order behavior is seen, which indicates that the state dynamics are closely coupled. Efficiency is approximately 95%. Two different approaches were then used to achieve the time-scale separation requirement.

First, additional resistance (2 Ω) was added in series with the inductor, which increased δ_0 to 0.026. Time-scale separation was achieved at the price of additional losses. Current and voltage waveforms for the same duty cycle step as above (67% to

TABLE 3.1. BASIC CONVERTER PARAMETERS.

L	657 μH	C	77 μF
R_L	584 $\text{m}\Omega$	R_C	381 $\text{m}\Omega$
MOSFET	IRF3710	Diode	MBR1545CT
ϵ	8.5×10^{-4}	δ_0	5.9×10^{-3}
Frequency	25 kHz	p	5.2×10^{-3}
R	100 Ω		

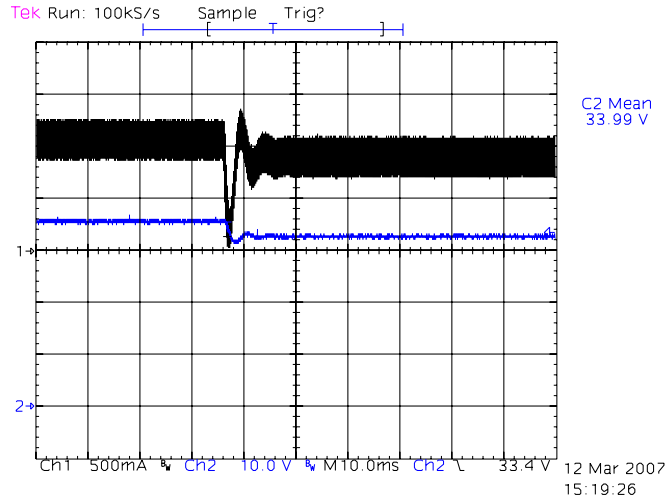


Fig. 3.2. Experimental duty cycle step (67% to 64%) with original converter. Note second-order behavior. Top waveform, channel 1, inductor current, 500 mA/div; bottom waveform, channel 2, output voltage, 10 V/div; horizontal, 10 ms/div.

64%) are shown in Fig. 3.3. More resistance would be needed for time-scale separation across a wide range of u . Efficiency was about 81%.

The additional losses are undesirable for a highly efficient power converter, so another approach was examined: additional capacitance. Figure 3.4 shows current and voltage trajectories for a smaller step, 67% to 66%, where the converter has an additional

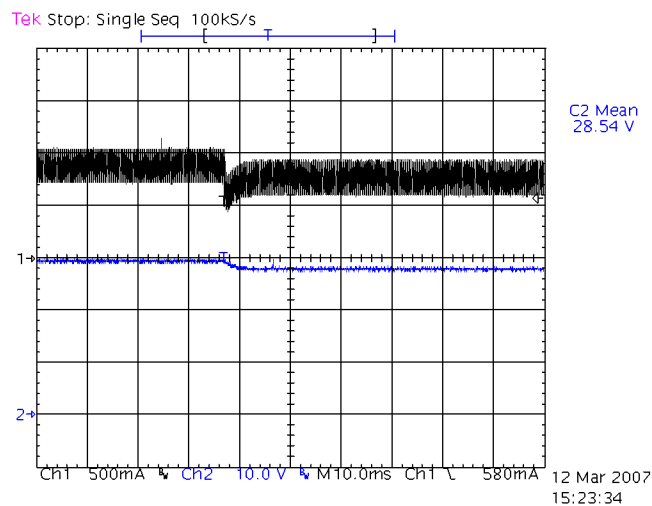


Fig. 3.3. Experimental duty cycle step (67% to 64%) with added resistance in inductor (2Ω). Top waveform, channel 1, inductor current, 500 mA/div; bottom waveform, channel 2, output voltage, 10 V/div; horizontal, 10 ms/div.

2200 μF to reduce ε to 3.16×10^{-5} and decrease p to 1.92×10^{-4} . The efficiency was still high, about 95%. However, dynamic performance suffered. The current response to a smaller input transient was larger and decayed more slowly. Figure 3.4 most clearly shows the factors that contribute to the approximate model. The rapid drop in current is mostly the off-manifold dynamics as η decays to zero, while the recovery towards the initial current is governed by the integral manifold as the voltage changes.

For the experimental converter, the KBM average can be numerically evaluated.

The leading coefficient of the \mathbf{G}_3 terms is

$$\frac{1}{12} \left(\frac{u(1-u)p}{\varepsilon} \right)^2 = 0.151 \quad (3.20)$$

As expected, continuous conduction mode corresponds to a leading coefficient less than unity. The most important element of the theoretical development is the η dynamic equation. For the three cases, the dynamic equations for η that include \mathbf{G}_3 terms are

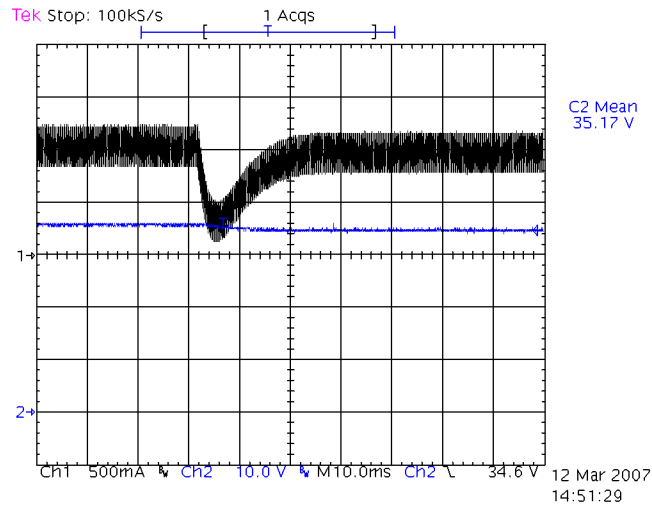


Fig. 3.4. Experimental duty cycle step (67% to 66%) with added output capacitance (2200 μF). Top waveform, channel 1, inductor current, 500 mA/div; bottom waveform, channel 2, output voltage, 10 V/div; horizontal, 10 ms/div.

$$\begin{aligned}
\varepsilon \left. \frac{d\eta}{d\hat{t}} \right|_{base} &= 6.99\eta - 2.60 \times 10^{-13} y_1 + 2.60 \times 10^{-13} w \\
\varepsilon \left. \frac{d\eta}{d\hat{t}} \right|_{add R} &= -27.9\eta - 2.43 \times 10^{-14} y_1 + 1.95 \times 10^{-13} w \\
\varepsilon \left. \frac{d\eta}{d\hat{t}} \right|_{add C} &= -210\eta - 1.21 \times 10^{-12} y_1 - 3.95 \times 10^{-12} w
\end{aligned} \tag{3.21}$$

In the base case, the coefficient of η is positive, so the approximate model is unstable and inappropriate. In the other two cases, the coefficients of η are negative as desired.

Notice also the orders of magnitude of the y_1 and w terms: Since y_1 and w are both $O(1)$, these small terms will only move the η equilibrium value a small distance from zero.

While z will not lie exactly on the integral manifold, the difference is negligible.

The analysis and experiments agree and show three possible cases. The base converter has fast, coupled dynamics and exhibits second-order behavior. One variant has higher losses with fast, decoupled dynamics. Another variant has additional capacitance for high efficiency and slow, decoupled dynamics.

3.3.5. Other load types

While the analysis above applies only to constant-resistance loads, there are two other static load types: constant-current and constant-power. If the load R is replaced with a Norton equivalent, all three load types can be included, at least in a small-signal sense. See Fig. 3.5 for the new configuration with I_N and R_N .

Generally, I_N is always non-negative, but R_N may be of either sign. If R_N is positive, the current sink moves the equilibrium by some offset. Off-manifold dynamics do not change. For a constant-current load, R_N approaches infinity and ε approaches zero, so the dynamical system is singular. For a constant-power load, I_N is positive and R_N is

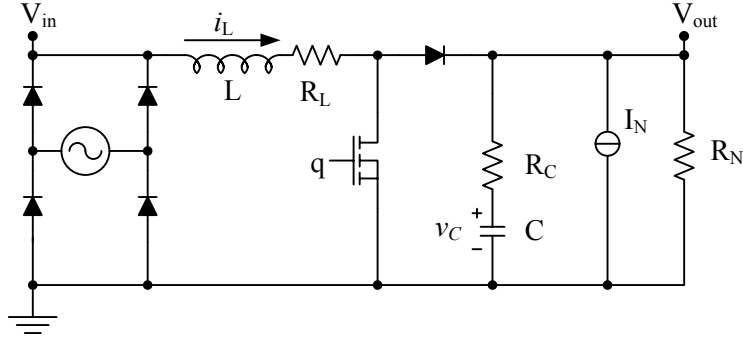


Fig. 3.5. Boost converter with Norton load.

negative, which changes the analysis. The normalized variables must be changed so that they have the same sign as the physical variables. Typically, $|R_N| > R_C$:

$$\begin{aligned}
 \hat{v}_C &= \frac{v_C}{V_0} \\
 \hat{i}_L &= -\frac{i_L R_N}{V_0} \\
 w_1 &= \frac{V_{in}}{V_0} \\
 w_2 &= -\frac{I_N R_N}{V_0} \\
 u &= \langle h_2 \rangle
 \end{aligned} \tag{3.22}$$

$$\begin{aligned}
 \hat{t} &= -\frac{t}{C(R_N + R_C)} \\
 p &= -\frac{T}{C(R_N + R_C)} \\
 \delta_0 &= \frac{R_L}{R_N} \frac{R_N + R_C}{R_N} \\
 \varepsilon &= \frac{L}{R_N^2 C}
 \end{aligned} \tag{3.23}$$

All variables are positive except δ_0 , which is negative. The dynamical equations change to

$$\frac{d}{dt} \begin{bmatrix} \hat{v}_C \\ \hat{i}_L \end{bmatrix} = \begin{bmatrix} 1 & h_2 \\ -\frac{h_2}{\varepsilon} & \frac{1}{\varepsilon} \left(\delta_0 + h_2 \frac{R_C}{R_N} \right) \end{bmatrix} \begin{bmatrix} \hat{v}_C \\ \hat{i}_L \end{bmatrix} + \begin{bmatrix} w_2 \\ \frac{1}{\varepsilon} \left(\frac{R_C + R_N}{R_N} w_1 - h_2 w_2 \frac{R_C}{R_N} \right) \end{bmatrix} \quad (3.24)$$

As above, KBM averaging converts this switched linear system into a nonlinear time-invariant system. Singular perturbation analysis yields an approximate model for the moving-average of \hat{i}_L , plus a differential equation that governs off-manifold dynamics.

$$\varepsilon \frac{d\eta}{dt} = \left(\delta(u) - \frac{u^2 \varepsilon}{\delta(u)} \right) \eta \quad (3.25)$$

Eq. (3.25) differs only slightly from (3.16). The small coefficient $\delta(u)$ is the same as above (3.13) and is negative. Time-scale separation requires stable η dynamics.

$$\delta(u) - \frac{u^2 \varepsilon}{\delta(u)} < 0 \quad (3.26)$$

With some algebraic manipulation, and with care for sign changes, the stability requirement reduces to

$$u^2 \varepsilon < \delta^2(u) \quad (3.27)$$

Simplifications can be applied as above and yield the same stability requirement as (3.19).

3.3.6. Experimental validation with constant power load

The converters described in Section 3.3.4 were tested with a constant power load. The load consisted of a large BJT (D44VH10), 57 Ω of resistive ballast, and a control circuit built around an AD633 analog multiplier. Integral control was used to regulate the power on a sub-millisecond time scale. The power was set to 13 W to correlate with the previous test points.

Figure 3.6 shows the response of the base converter with a constant power load. As in Fig. 3.2, the dynamics resemble a second-order system. For Fig. 3.7, an extra $2\ \Omega$ was inserted in series with the inductor for fast, decoupled dynamics. For a constant power load, converter efficiency dramatically impacts output voltage. For Fig. 3.8, an extra $1400\ \mu\text{F}$ was added instead of the resistance. High efficiency is retained, while the response time is increased.

To summarize, time scale separation can be achieved for any load that includes a resistive term, whether the resistance is positive or negative. Typically, the inductor will be designed to satisfy ripple current and efficiency requirements. Given the corresponding L and R_L , the designer can choose the capacitor to satisfy (3.19) and separate voltage and current time scales.

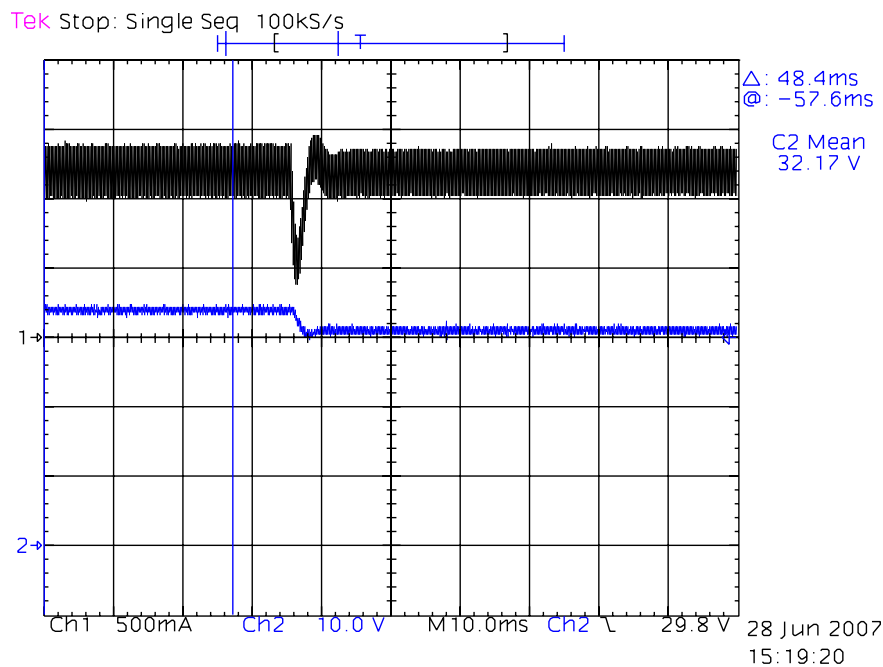


Fig. 3.6. Experimental duty cycle step (67% to 64%) with original converter, now with a constant-power load. Top waveform, channel 1, inductor current, 500 mA/div; bottom waveform, channel 2, output voltage, 10 V/div; horizontal, 10 ms/div.

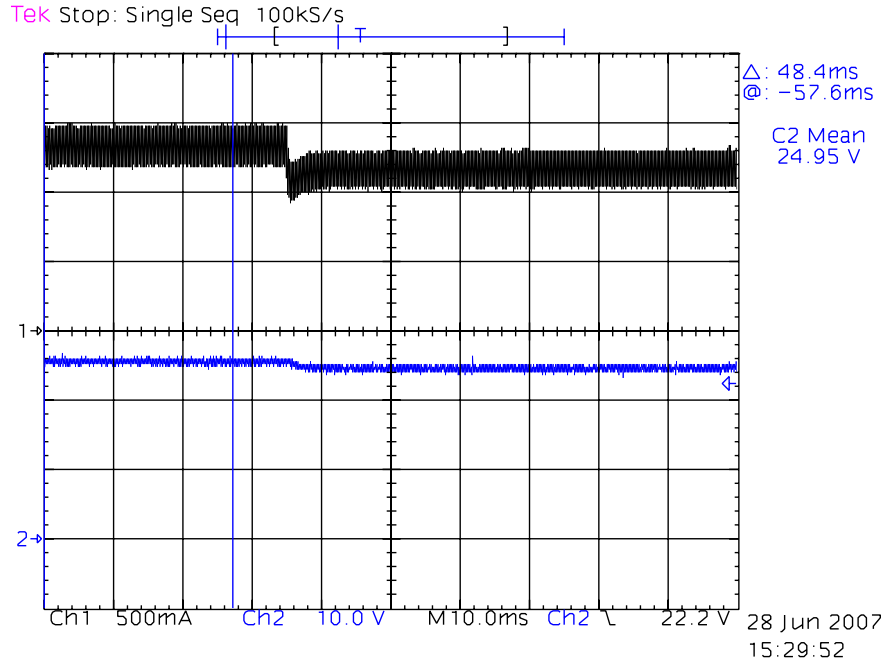


Fig. 3.7. Experimental duty cycle step (67% to 64%) with increased resistance and constant power load. Top waveform, hannel 1, inductor current, 500 mA/div; bottom waveform, channel 2, output voltage, 10 V/div; horizontal, 10 ms/div.

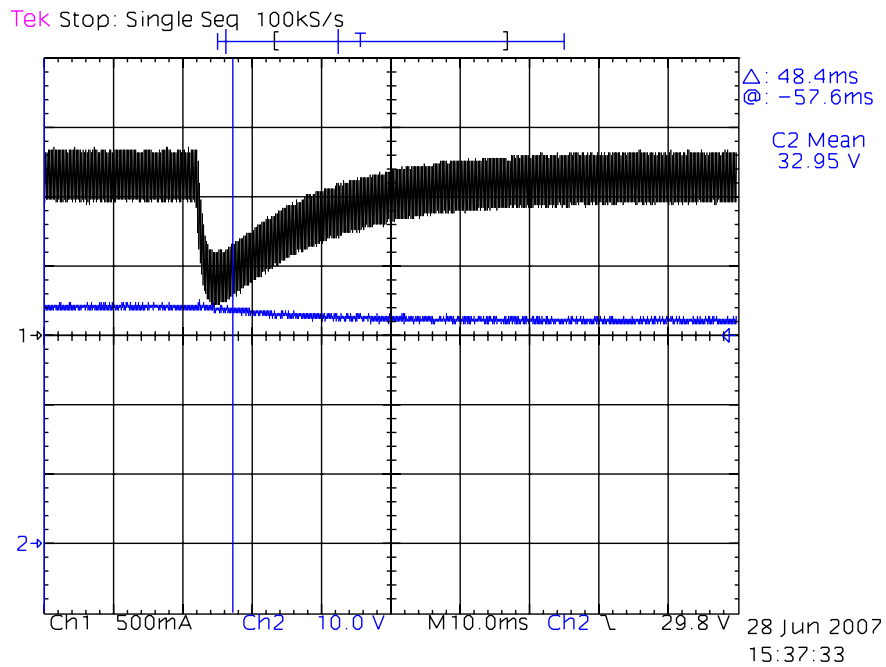


Fig. 3.8. Experimental duty cycle step (67% to 65%) with increased capacitance and constant power load. Top waveform, channel 1, inductor current, 500 mA/div; bottom waveform, channel 2, output voltage, 10 V/div; horizontal, 10 ms/div.

3.4. Other Converter Types

3.4.1. Buck and buck-boost converters

Boost, buck, and buck-boost converters all are composed of the same elements—one inductor, one capacitor, one controlled switch, and one diode each. For clarity, the same normalized variable definitions of (3.5)-(3.6) will be used in the analysis of buck and buck-boost converters.

A buck converter, shown in Fig. 1.1, has dynamics that are time-invariant in the states. In the KBM average, all terms above \mathbf{G}_1 vanish. The normalized, averaged model in singular perturbation standard form is

$$\begin{aligned}\frac{dx}{d\hat{t}} &= z - x \\ \varepsilon \frac{dz}{d\hat{t}} &= \frac{R + R_c}{R} (1 - u) w - x - \left(\delta_0 + \frac{R_c}{R} \right) z\end{aligned}\tag{3.28}$$

The similarities between (3.28) and (3.12) are obvious. As might be expected, then, the approximate model for z is similar to the boost converter case, with off-manifold dynamics governed by

$$\varepsilon \frac{d\eta}{d\hat{t}} = \left(\frac{\varepsilon}{\delta_0} - \delta_0 \right) \eta\tag{3.29}$$

The η dynamics are stable for

$$\varepsilon < \delta_0^2\tag{3.30}$$

As in the boost converter case, simplifications can be made that result in exactly the same criterion as (3.19).

The buck-boost converter shown in Fig. 3.9 has dynamics that are time-varying in the states, similar to a boost converter. Considering only the state space average (\mathbf{G}_1), the normalized dynamics are

$$\begin{aligned} \frac{dx}{d\hat{t}} &= uz - x \\ \varepsilon \frac{dz}{d\hat{t}} &= \frac{R + R_C}{R} (1-u) w - ux - \left(\delta_0 + \frac{R_C}{R} u \right) z \end{aligned} \quad (3.31)$$

Again, similarities to the boost converter model are obvious. In fact, the η dynamic equation is identical to that of the boost converter (3.16), so the stability criterion is identical to (3.19). \mathbf{G}_3 can be considered numerically and has a similar effect on η as in a boost converter.

3.4.2. Flyback converter

A flyback converter is an isolated buck-boost converter. Where a buck-boost converter has a simple inductor, a flyback converter has a coupled inductor. The isolation can be used to reverse the voltage inversion inherent to a buck-boost converter, and a turns-ratio can change the overall conversion ratio. A simplified schematic is shown in Fig. 3.10.

The time-varying (switched system) dynamics of a flyback converter require a

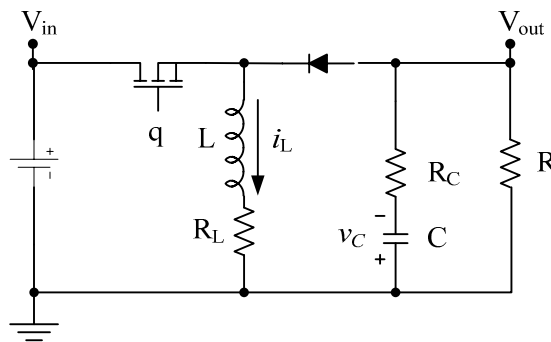


Fig. 3.9. Buck-boost converter.

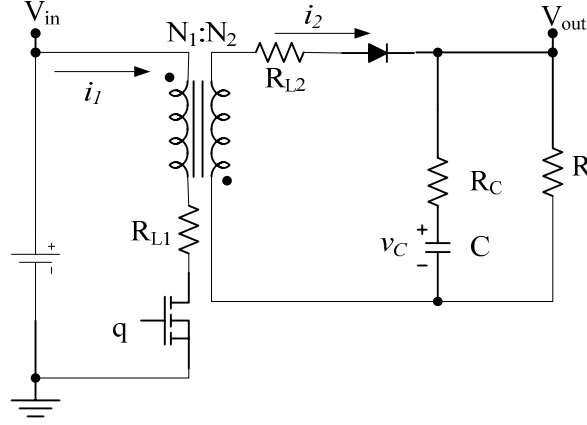


Fig. 3.10. Flyback converter.

few new variables. As above, v_C is the capacitor voltage and h_2 is a Boolean variable that is true when the diode is conducting. Similarly, h_1 is a Boolean variable that is true when the controlled switch is turned on. We will assume continuous conduction mode, meaning that either the controlled switch or the diode is conducting at all times. The coupled inductor has permeance \mathcal{P} , and the flux in the core is ϕ . Leakage flux is neglected to give time-varying system dynamics:

$$\begin{aligned} \frac{dv_C}{dt} &= -\frac{v_C}{C(R+R_C)} + \frac{R}{C(R+R_C)} \frac{h_2}{N_2 \mathcal{P}} \phi \\ \frac{d\phi}{dt} &= h_1 \left(\frac{V_{in}}{N_1} - \frac{R_{L1}}{N_1^2 \mathcal{P}} \phi \right) + h_2 \left(-\frac{R}{R+R_C} \frac{v_C}{N_2} - \frac{R_{L2} + (R \parallel R_C)}{N_2^2 \mathcal{P}} \phi \right) \end{aligned} \quad (3.32)$$

Since there are new variables, the normalization process is slightly different. The normalized variables are

$$\begin{aligned} \hat{v}_C &= \frac{v_C}{V_0} \\ \hat{\phi} &= \frac{\phi}{N_2 \mathcal{P} V_0} \\ w &= \frac{V_{in}}{V_0} \frac{N_2}{N_1} \\ d &= \langle h_1 \rangle \\ u &= 1 - d = \langle h_2 \rangle \end{aligned} \quad (3.33)$$

$$\begin{aligned}
\hat{t} &= \frac{t}{C(R+R_C)} \\
p &= \frac{T}{C(R+R_C)} \\
\varepsilon &= \frac{N_2^2 \mathcal{P}}{R^2 C} \\
\hat{R}_{L1} &= R_{L1} \left(\frac{N_2}{N_1} \right)^2
\end{aligned} \tag{3.34}$$

There is no convenient definition of δ_0 , although $\delta(u)$ will appear below. With these definitions in place (3.33)-(3.34), the normalized, state-space-averaged dynamical system becomes

$$\begin{aligned}
\frac{d\hat{v}_C}{d\hat{t}} &= -\hat{v}_C + u\hat{\phi} \\
\varepsilon \frac{d\hat{\phi}}{d\hat{t}} &= \frac{R_C + R}{R} (1-u)w - u\hat{v}_C - \delta(u)\hat{\phi} \\
\delta(u) &= \frac{R_C + R}{R} \left(\hat{R}_{L1} (1-u) + uR_{L2} \right) + u \frac{R_C}{R}
\end{aligned} \tag{3.35}$$

A close comparison of (3.35) and (3.31) reveals that a continuous-mode flyback converter and a continuous-mode buck-boost converter have identical dynamics, although with slightly different loss mechanisms. The fast state variable is the flux ϕ , rather than a current. In a conventional coupled-inductor design, $\hat{R}_{L1} = R_{L2}$, so the new definition of $\delta(u)$ simplifies to the definition given for boost and buck-boost converters (3.13).

To demonstrate the results of both the buck-boost analysis and flyback converter analysis, a simple flyback converter with a 1:1 coupled inductor was constructed. Converter parameters were similar to the boost converter described above (same MOSFET and diode). Each coil of the coupled inductor was 658 μH with 256 $\text{m}\Omega$ of

resistance. The output capacitor was 170 μF with 141 $\text{m}\Omega$ of equivalent series resistance (ESR). A resistive load (100 Ω) was applied.

There are two state variables to probe, v_C and ϕ . Unfortunately, ϕ is extremely difficult to measure. While the controlled switch is conducting, $\phi = \frac{N_1 i_1}{\mathcal{P}}$, so the envelope of i_1 gives an indication of the dynamics of ϕ . Figure 3.11 shows flyback converter dynamics for a duty cycle step. As in the base case for the boost converter, the dynamics are coupled and second-order behavior is evident.

There are two methods for achieving time-scale separation. Figure 3.12 shows the dynamics that result from increased series resistance (an additional 2 Ω). Figure 3.13 shows the dynamics that result from increased output capacitance (an additional 1400 μF). Increased resistance greatly impacts output voltage, while increased capacitance slows down the overall response.

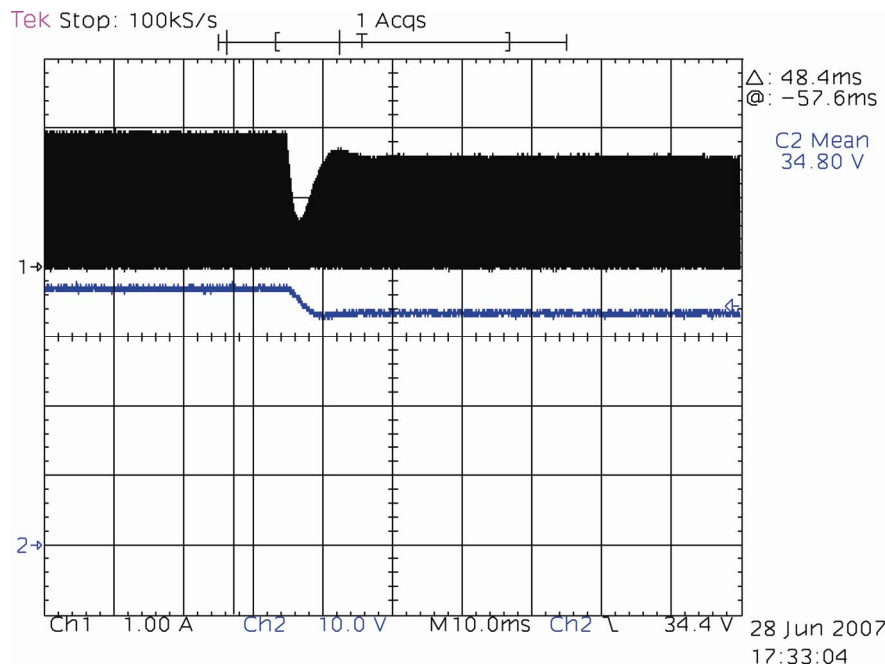


Fig. 3.11. Experimental duty cycle step (75% to 73%) with original flyback converter. Top waveform, channel 1, primary current, 1 A/div; bottom waveform, channel 2, output voltage, 10 V/div; horizontal, 10 ms/div.

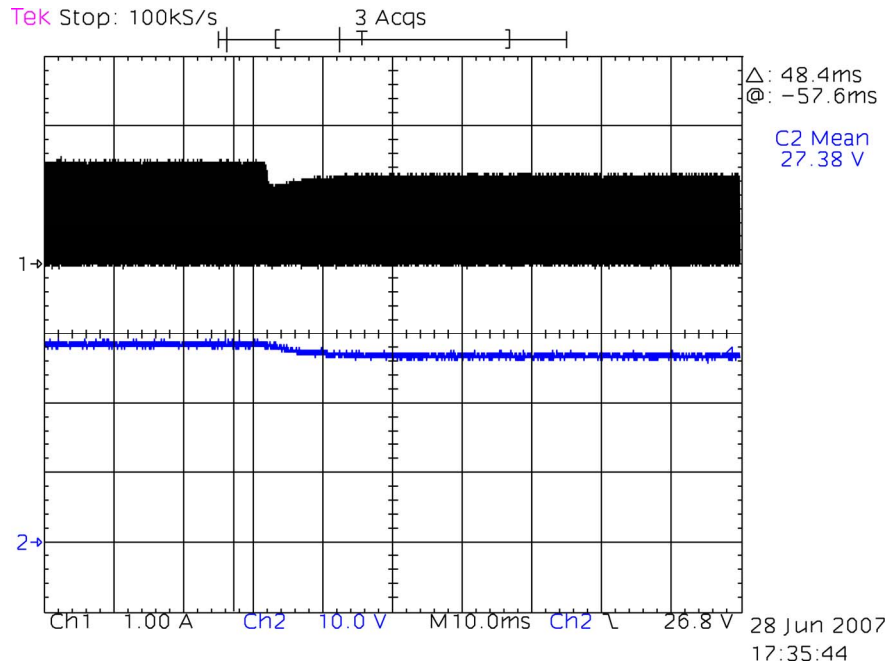


Fig. 3.12. Experimental duty cycle step (75% to 73%) with increased primary-side resistance. Top waveform, channel 1, primary current, 1 A/div; channel 2, output voltage, 10 V/div; horizontal, 10 ms/div.

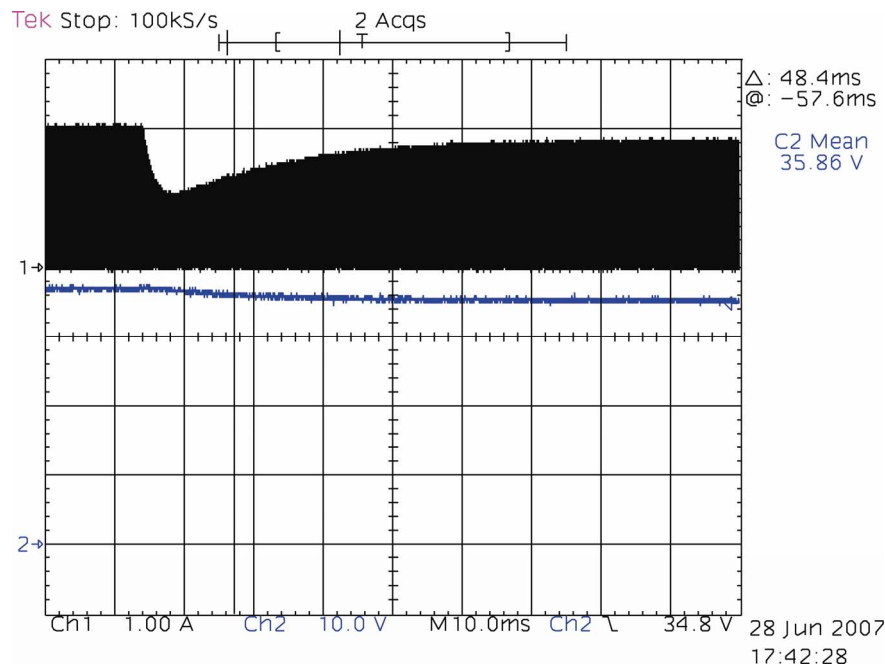


Fig. 3.13. Experimental duty cycle step (75% to 74%) with increased output capacitance. Top waveform, channel 1, primary current, 1 A/div; bottom waveform, channel 2, output voltage, 10 V/div; horizontal, 10 ms/div.

3.5. Sampled-Data (Discrete-Time) Analysis

Digital controllers operate in discrete time, whereas the preceding sections analyze power converters in continuous time. A sampled-data model [4, 18] can be similarly analyzed for time-scale separation. Just as in the continuous-time domain, generic discrete-time systems have been analyzed with singular perturbation theory [181-185].

The boost converter of Fig. 3.1 demonstrates the basic problem of time-scale separation. First, the continuous-time model of (3.7) needs to be converted to discrete-time. For notational convenience, rewrite the continuous-time model as

$$\begin{aligned} \frac{d}{dt} \begin{bmatrix} \hat{v}_C \\ \hat{i}_L \end{bmatrix} &= (\mathbf{A}_1 + h_2 \mathbf{A}_2) \begin{bmatrix} \hat{v}_C \\ \hat{i}_L \end{bmatrix} + \mathbf{B}_1 w \\ \mathbf{A}_1 &= \begin{bmatrix} -1 & 0 \\ 0 & -\frac{\delta_0}{\varepsilon} \end{bmatrix} \\ \mathbf{A}_2 &= \begin{bmatrix} 0 & 1 \\ -\frac{1}{\varepsilon} & -\frac{R_C}{\varepsilon R} \end{bmatrix} \\ \mathbf{B} &= \begin{bmatrix} 0 \\ \frac{R_C + R}{\varepsilon R} \end{bmatrix} \end{aligned} \tag{3.36}$$

With the input voltage (equivalently, w) and duty cycle (or u) held constant for one cycle p (in normalized time), the discrete-time system can be written as

$$\begin{aligned}
\begin{bmatrix} \hat{v}_c \\ \hat{i}_L \end{bmatrix}[k+1] &= \mathbf{\Phi}[k] \begin{bmatrix} \hat{v}_c \\ \hat{i}_L \end{bmatrix}[k] + \mathbf{\Gamma}[k] w[k] \\
\mathbf{\Phi}[k] &= \exp(\mathbf{A}_1(1-u[k])p) \exp((\mathbf{A}_1 + \mathbf{A}_2)u[k]p) \\
\mathbf{\Gamma}[k] &= \frac{\mathbf{A}_1^{-1}}{(1-u[k])p} \left(\exp(\mathbf{A}_1(1-u[k])p) - \mathbf{I} \right) \mathbf{B}w[k] \\
&\quad + \frac{(\mathbf{A}_1 + \mathbf{A}_2)^{-1}}{u[k]p} \left(\exp((\mathbf{A}_1 + \mathbf{A}_2)u[k]p) - \mathbf{I} \right) \mathbf{B}w[k]
\end{aligned} \tag{3.37}$$

The contribution from the input voltage does not enter into the remaining discussion.

The state transition matrix $\mathbf{\Phi}$ can be approximated since

$$\exp(\mathbf{A}t) = \mathbf{I} + \mathbf{A}t + O((\mathbf{A}t)^2) \tag{3.38}$$

Discarding all terms quadratic in time p ,

$$\mathbf{\Phi}[k] \approx (\mathbf{I} + \mathbf{A}_1(1-u[k])p)(\mathbf{I} + (\mathbf{A}_1 + \mathbf{A}_2)u[k]p) \tag{3.39}$$

Then we expand (3.39), substitute the actual values of \mathbf{A}_1 and \mathbf{A}_2 , and again discard all terms quadratic in p .

$$\mathbf{\Phi}[k] \approx \begin{bmatrix} 1-p & u[k]p \\ -\frac{u[k]p}{\varepsilon} & 1 - \frac{u[k]p}{\varepsilon} \frac{R_c}{R} - \frac{p\delta_0}{\varepsilon} \end{bmatrix} \tag{3.40}$$

The approximated state transition matrix does not satisfy the criteria in [181]. However, at the least we may check whether the eigenvalues are real and distinct, rather than complex conjugate. If so, then there is moderate time-scale separation.

The eigenvalues of $\mathbf{\Phi}$ (as approximated in (3.40), and with the time index k implicit) are

$$1 + \frac{p}{2\varepsilon} \left(u \frac{R_C}{R} + \delta_0 \right) + \frac{p}{2} \pm \sqrt{DISCRIMINANT}$$

$$DISCRIMINANT = \frac{p^2}{4\varepsilon^2} \left(\left(\frac{R_C}{R} u + \delta_0 - \varepsilon \right)^2 - 4u^2\varepsilon \right)$$
(3.41)

The eigenvalues will be real and distinct if

$$DISCRIMINANT > 0$$
(3.42)

With (3.41) substituted into (3.42),

$$\left(\frac{R_C}{R} u + \delta_0 - \varepsilon \right)^2 > 4u^2\varepsilon$$
(3.43)

will guarantee real, distinct roots. As in the continuous-time case, simplifying approximations can be made. The most conservative bound, analogous to (3.19), is

$$R_L > 2\sqrt{\frac{L}{C}}$$
(3.44)

The experimental boost converter of Section 3.3.4 can be analyzed in discrete time. A summary of results is shown in Table 3.2. In general, the conservative bound of (3.44) is too conservative, if modest time-scale separation is allowable.

Faster switching generally leads to less separation, since p^2 is a significant factor in the discriminant. From another perspective, a lower sampling rate leads to more separation. Although the sampled-data model presented here presumes a sampling rate

TABLE 3.2. EXPERIMENTAL BOOST CONVERTER IN SAMPLED-DATA FRAMEWORK.

Experimental Case	Eqn. (3.44)?	Eqn. (3.43)?	Eigenvalues
Base	0.584 < 5.8421 NO	3.93e-5 < 3.72e-4 NO	0.9761 ± j0.0554
Add 2 Ω to R _L	2.584 < 5.8421 NO	6.94e-4 > 3.72e-4 YES	0.9678, 0.8684
Add 2.2 mF to C	0.584 < 1.0743 NO	5.03e-5 > 1.26e-5 YES	0.9969, 0.9602

equal to the switching frequency, this need not be the case. If the eigenvalues are real and distinct, even a small difference will become substantial over many switching cycles. For example, for the case where additional resistance is added in series with the inductor, the eigenvalues of Φ for a 25 kHz switching frequency are $\{0.9678, 0.8684\}$. If both the switching frequency and sampling rate are increased to 250 kHz, the eigenvalues are $\{0.9969, 0.9861\}$ —a small difference. If the sampling rate is left at 25 kHz but the switching frequency is set to 250 kHz, the eigenvalues are $\{0.9697, 0.8696\}$ —nearly the same as with 25 kHz switching. Over the range where the converter remains in continuous conduction mode, increased switching frequency narrows the apparent difference between time scales, while separation is retained if sampling rate remains constant regardless of switching frequency.

3.6. Relationship to Middlebrook Stability Requirement

The ratio between a power converter’s output impedance and its load’s input impedance determines whether the combination is stable. The seminal work by Middlebrook [186] established a conservative, sufficient condition for system stability. Given a power converter with complex output impedance Z_o and a load with complex input impedance Z_i , the system will be stable if

$$|Z_o| < |Z_i| \quad (3.45)$$

at all frequencies. Although less conservative requirements have been proposed, the requirement in (3.45) is adequate for the present analysis. A switching power converter can be modeled as a constant power load, so the Norton equivalent circuit analysis of Section 3.3.5 applies here.

To reveal any relationship between the preceding analysis and the stability requirement, we must examine Z_o . According to [186], the output impedance of a boost converter is just as in a buck converter, with an equivalent inductance of $L_e = L/u^2$ and an equivalent resistance $R_e = R_L/u^2$.

$$\begin{aligned}
 Z_o &= (R_e + sL_e) \parallel \left(R_C + \frac{1}{sC} \right) \\
 &= \frac{R_L}{u^2} \frac{1 + s \left(\frac{L}{R_L} + R_C C \right) + s^2 \left(LC \frac{R_C}{R_L} \right)}{1 + sC \left(\frac{R_L}{u^2} + R_C \right) + s^2 \left(\frac{LC}{u^2} \right)}
 \end{aligned} \tag{3.46}$$

This form of Z_o is typically compared to Z_i with a Bode plot. A conventional design will easily satisfy (3.45) at dc, so the only concern is whether Z_o increases at some frequency and exceeds Z_i .

Although (3.46) cannot be simplified further without numerical component values, the presence or absence of resonance can be determined easily. If the denominator has complex roots, the impedance will rise substantially at the resonant frequency (approximately $\omega_o = 1/\sqrt{LC}$). To guarantee distinct, real roots,

$$4LCu^2 < (R_L C + R_C C u^2)^2 \tag{3.47}$$

This conservative stability requirement can be put into a form that resembles the singular perturbation analysis. Divide through by $R_N^2 C$ to find

$$4u^2 \varepsilon < \left(\frac{R_L + R_C u^2}{R_N} \right)^2 \tag{3.48}$$

This form does not quite correlate to any of the preceding analysis. However, some similarities to the sampled-data model analysis are apparent. Equation (3.43) can be manipulated into

$$4u^2 \varepsilon < \left(\frac{R_L + uR_C + \frac{R_L R_C}{R} - \frac{L}{RC}}{R} \right)^2 \quad (3.49)$$

In practical terms, most converters that satisfy one of the singular perturbation requirements will also satisfy the Middlebrook stability requirement (3.45) over all frequencies. For example, Bode plots of Z_o and Z_i are shown in Fig. 3.14 for the converter scenarios described in Section 3.3.6. In all cases, the combined system is stable. In the base case, resonance is observed, although the impedance is still low. For the other two cases, no resonance occurs. A converter with more resistance in the inductor has higher impedance overall, which again pushes a designer towards additional capacitance.

3.7. Conclusions

Singular perturbation analysis of buck, boost, buck-boost, and flyback converters explicitly determined criteria for time-scale separation of inductor current and capacitor voltage dynamics. An experimental boost converter demonstrated a base design with no decoupling and two approaches to achieve the decoupling. Additional losses allow the converter to retain fast dynamics, while additional capacitance allows the converter to retain high efficiency. Similar conclusions apply to buck, buck-boost, and flyback converters. An experimental flyback converter showed the effect of design choices on a buck-boost-derived converter.

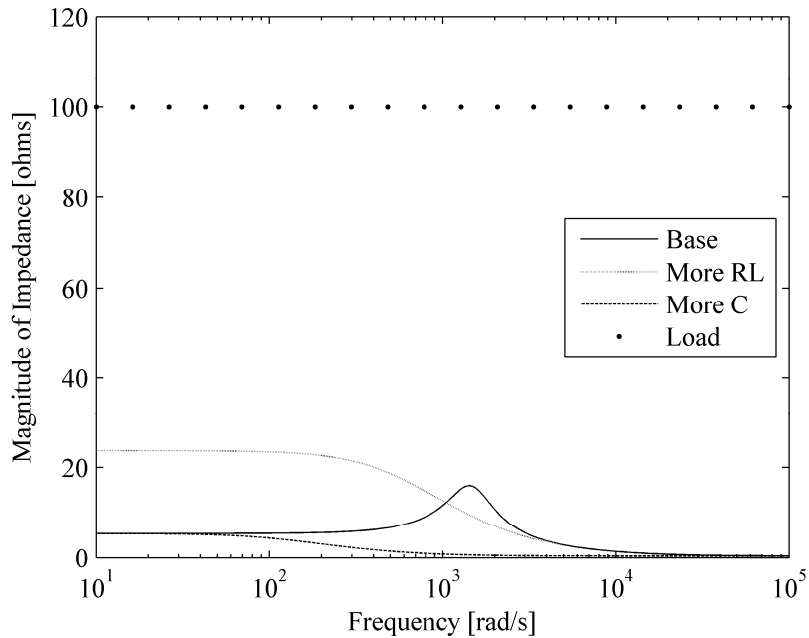


Fig. 3.14. Comparison of output impedances and load impedance for the experimental converters of Section 3.3.6.

Future work should study the form of u , the control input. In the development here, u was assumed to be exogenous, so only the open-loop plant dynamics were considered. In a typical converter, though, u is determined from the states (and possibly the disturbance input). The feedback law often includes additional states. For example, integral control is common. This additional complication may or may not affect the time-scale separation shown here. Another topic of interest is discontinuous conduction mode operation.

While many applications of singular perturbation theory seek to eliminate the fast time scale from control design or system analysis, the fast time scale is critical in power electronics. The next two chapters discuss applications that use information from the fast time scale to attain some control objective. In Chapter 4, fast time scale information is used to control current, also at the fast time scale, regardless of voltage. In Chapter 5, fast time scale information is used to shift the steady-state operating point, on the slow

time scale, to an optimum. Other future work could consider existing applications that use fast time scale information, such as peak current mode control.

CHAPTER 4

DIGITAL EFFECTS AND KALMAN FILTERS

There are two major differences between digital controllers and analog controllers: all digital system inputs and outputs are sampled and quantized. Prior work on the effects of these two mechanisms [187-189] has shown that finite resolution in time and in value can give rise to limit cycles and other undesirable phenomena. However, sampling can also be used to advantage in control design. For example, sampling current at the correct time can allow direct control of peak, valley, or average current in predictive current control [45]. In the present chapter, the objective is to mitigate sampling effects with Kalman filters [53], while the following chapter will use precise sample timing for control purposes.

A Kalman filter is similar to an observer, except that the basic framework is stochastic rather than deterministic. Like observers, Kalman filters can be used to augment or replace sensors. While an observer is an excellent choice if the noise in the system is small, Kalman filters are preferable in switching power converters for two reasons. First, the noise may not be small, particularly when there is a large analog gain or attenuation between the physical plant and the controller. Second, most power converters have high current gain. A small voltage deviation can cause a large current transient, which in turn can be destructive or can cause a large voltage transient. A Kalman filter inherently compensates for noise in the system and can mitigate excessive transients.

A Kalman filter is an estimator for states in a dynamical system that has additive noise in both state dynamics and output sensing. If the noise is Gaussian and all samples

are independent, then the estimate will be optimal in a mean-square sense; that is, the variance of the estimator error will be at a minimum. If the noise takes some other form, then a Kalman filter will provide the best estimate that can be obtained with linear feedback. Typically, Kalman filters are used for signal processing purposes, such as for interpreting radar results. They are often used where some dynamics are known while external influences are unknown. In the present work, all state transition matrices are the identity matrix, so that external influences dominate. While continuous-time versions are possible, the present work uses the prevalent discrete-time version.

Section 4.1 gives background on Kalman filters and extended Kalman filters (EKFs). Section 4.2 applies Kalman filters to the problem of ac voltage sensing in a PFC converter. Section 4.3 expands on this basic framework and shows Kalman filters used in a controller. Section 4.4 summarizes the benefits and future potential of Kalman filters for digital control of switching power converters.

4.1. Background on Kalman Filters and Extended Kalman Filters

A Kalman filter is similar to a discrete-time observer. A plant model is constructed with one or more discrete state variables and an output equation. An estimator uses the same plant model to generate estimated state variables. Feedback on the error between actual and estimated output corrects the state estimates.

The basic difference is that Kalman filters are built on stochastic assumptions, rather than deterministic assumptions. The standard plant model is

$$\mathbf{x}[k] = \mathbf{\Phi}[k-1]\mathbf{x}[k-1] + \mathbf{\Gamma}[k-1]\mathbf{w}[k-1] \quad (4.1)$$

In general, \mathbf{x} is a vector of n discrete state variables with time index k . The term $\mathbf{\Phi}$ is the state transition matrix, which may be time-varying. The term $\mathbf{\Gamma}$ accumulates the effects

of all known (deterministic) inputs. The last component, \mathbf{w} , is a random process with zero mean and covariance matrix \mathbf{Q} . A Kalman filter is optimal if each sample of \mathbf{w} is Gaussian and independent. If \mathbf{w} takes some other form, a Kalman filter is still the best linear estimator.

There are two possible output equation forms that result in either conventional or extended Kalman filters. A conventional Kalman filter assumes a linear output equation,

$$\mathbf{z}[k] = \mathbf{H}[k]\mathbf{x}[k] + \mathbf{v}[k] \quad (4.2)$$

The output \mathbf{z} is a vector of length m . \mathbf{H} is an $m \times n$ matrix that may be time-varying. The added term, \mathbf{v} , is a random process with zero mean and covariance matrix \mathbf{R} . The two random processes \mathbf{w} and \mathbf{v} are uncorrelated. In the other system form, the output equation is nonlinear,

$$\mathbf{z}[k] = h(\mathbf{x}[k]) + \mathbf{v}[k] \quad (4.3)$$

If there are any system nonlinearities, the filter is termed an EKF. The filter itself is unchanged, except that the local derivative of $h(\mathbf{x})$ is needed.

$$\mathbf{H}[k] = \left. \frac{\partial h}{\partial \mathbf{x}} \right|_{\mathbf{x}=\mathbf{x}[k]} \quad (4.4)$$

So what are the states \mathbf{x} ? A power electronics expert might expect capacitor voltages or inductor currents to be the states. This need not be the case, though. In the examples below, the state variables are parameters that can be used to create a waveform—magnitude and phase information. Kalman filters can be considered as signal processing elements that extract useful information from noisy measurements. Kalman filter application relies on an appropriate system formulation that uses this

information in a controller, which may be significantly different from a conventional observer-based system.

An EKF can be designed for the dynamical system (4.1), with output equation (4.3) and derivative matrix (4.4). The filter tracks the covariance of the estimator error \mathbf{P} to determine the optimal gain \mathbf{K} . At each sample, an intermediate estimate of the new estimate covariance is computed from the dynamics of the state variables.

$$\mathbf{P}^- [k] = \Phi [k-1] \mathbf{P} [k-1] \Phi^T [k-1] + \mathbf{Q} [k-1] \quad (4.5)$$

Next, the optimal gain is computed from knowledge of the output equation.

$$\mathbf{K} [k] = \mathbf{P}^- [k] \mathbf{H}^T [k] (\mathbf{H} [k] \mathbf{P}^- [k] \mathbf{H}^T [k] + \mathbf{R} [k])^{-1} \quad (4.6)$$

The gain is used to update the state estimate $\hat{\mathbf{x}}$:

$$\hat{\mathbf{x}} [k] = \Phi [k] \hat{\mathbf{x}} [k-1] + \Gamma [k-1] + \mathbf{K} [k] (z [k] - h(\hat{\mathbf{x}} [k-1])) \quad (4.7)$$

Also, the error covariance is updated with the optimal gain.

$$\mathbf{P} [k] = (\mathbf{I} - \mathbf{K} [k] \mathbf{H} [k]) \mathbf{P}^- [k] \quad (4.8)$$

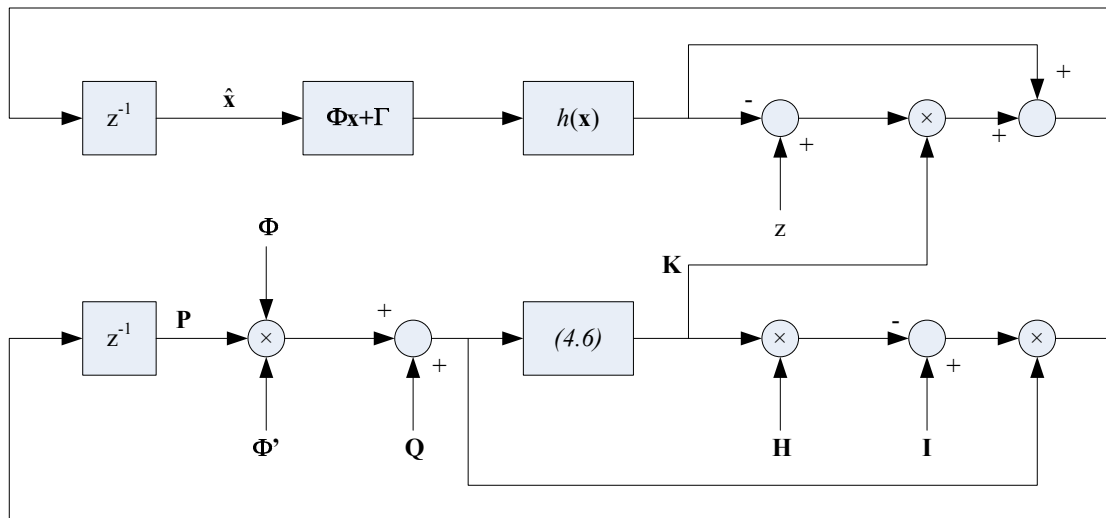


Fig. 4.1. Block diagram of standard extended Kalman filter process.

Then $\hat{\mathbf{x}}$ will converge to \mathbf{x} despite the presence of noise. The process is shown schematically in Fig. 4.1.

Practical implementation must overcome several issues. The plant model must have suitable states whose deterministic evolution can be established. Covariance matrices \mathbf{Q} and \mathbf{R} must be estimated, often from experimental data, simulations, or simple models. The estimator error covariance matrix \mathbf{P} must be initialized to a reasonable value.

EKFs, though computationally expensive, are tractable with readily available microprocessors. In addition to matrix multiplications, there is a matrix inversion and a nonlinear function h . For the present work, two EKFs were simultaneously implemented on a Texas Instruments TMS320F2812, which is a 32-bit fixed-point digital signal processor (DSP) that can achieve 133 MIPS [190]. In the experimental system, a clock speed of 75 MHz supported a 25 kHz update rate. Designers must have an awareness of computational complexity when formulating the system. The system described below in Section 4.3 uses two separate EKFs of two and three state variables, rather than one system with five state variables, to reduce the computations required for matrix inversion.

4.2. Application of an EKF to AC Voltage Sensing

In this section, an EKF will be developed for ac voltage sensing. The end application is a PFC converter, such as the boost converter of Fig. 3.1. In most PFC controllers, the input voltage V_{in} is sensed after the rectifier. Sample rate is limited, and sample values are quantized. Additionally, there is significant analog noise. The objective of the EKF is to produce an estimate of the true V_{in} , so that a PFC converter will produce clean, sinusoidal input current.

A Kalman filter can be constructed to determine the true input voltage magnitude and phase in the presence of quantization and analog noise. V_{in} is modeled as a sine wave. An external circuit generates a digital signal that gives the polarity of the ac voltage. If two successive samples of this digital polarity indicator differ, then a zero crossing has occurred and time is reset to zero. However, there may be an error between the actual zero crossing and the sensed zero crossing of as much as T , the sample period. This error, called θ and measured in radians, is based on the known radian line frequency ω (in the U.S., $\omega = 2\pi 60$ rad/s). A zoomed view of a typical zero crossing event is shown in Fig.

4.2. The output equation is

$$V_{in}[k] = V_{pk}[k] \sin(k\omega T + \theta[k]) + v[k] \quad (4.9)$$

The additive noise v will be discussed later. For this form of the output equation, the relevant states are V_{pk} and θ . So the dynamical system is

$$\begin{bmatrix} V_{pk} \\ \theta \end{bmatrix} [k] = \begin{bmatrix} V_{pk} \\ \theta \end{bmatrix} [k-1] + \mathbf{w}[k-1] \quad (4.10)$$

The state transition matrix is the identity matrix, that is, there are no deterministic dynamics. The magnitude and phase may drift between zero-crossings, though. Since the drift is nondeterministic, it can be modeled with a random variable \mathbf{w} .

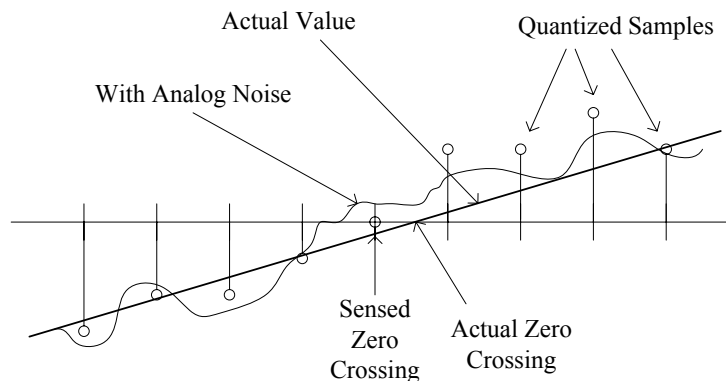


Fig. 4.2. Effects of analog noise and quantization on zero crossing detection.

There are two components to the sensed random variable v . The real value of V_{in} passes through an analog gain stage (gain G_v) which has some analog noise. Measurements of a physical system can give an indication of the magnitude of the analog noise. The noisy analog signal is then quantized by an ADC. Quantization noise can be calculated directly. The ADC has a resolution of p bits; for example, a TMS320F2812 has a 12-bit ADC. All signals must fit within the allowable input range $[0, V_{ADC}]$. So the quantization error e_q is limited to

$$-\frac{V_{ADC}}{G_v} \times \frac{1}{2^{p+1}} \leq e_q < \frac{V_{ADC}}{G_v} \times \frac{1}{2^{p+1}} \quad (4.11)$$

The quantization error e_q is a uniform random variable with zero mean and extends per (4.11), so the variance is

$$\sigma_{e_q}^2 = \frac{1}{3} \left(\frac{V_{ADC}}{2^{p+1} G_v} \right)^2 \quad (4.12)$$

In a typical system, analog noise dominates. A 12-bit ADC with $V_{ADC} = 2.5$ V and $G_v = 0.01$ gives a variance of 0.00031 V². Analog noise might be as much as 1% of full scale, or 2.5 V, for a variance of 6.25 V².

The other random process \mathbf{w} determines changes in V_{in} . The derivative of V_{pk} is governed by \mathbf{w}_1 . Experimentally, any small positive number used for the variance of \mathbf{w}_1 produces acceptable results, since line voltage changes over the course of minutes or hours and the sample rate is on the order of milliseconds. The angle θ is reset to its mean, $\frac{\omega T}{2}$, at each zero crossing. Since this time-quantization error is a uniform random variable ($\theta \in [0, \omega T]$), the corresponding term in the \mathbf{P} matrix is reset to

$$\mathbf{P}_{22} = \frac{(\omega T)^2}{12} \quad (4.13)$$

at each sensed zero crossing. The variance of \mathbf{w}_2 , which governs changes in θ over a cycle, must be smaller; an experimental value of $\frac{\mathbf{P}_{22}}{12}$ resulted in good performance.

This EKF was used effectively in the experimental PFC converter described in the next section. One drawback to the formulation of (4.9) is that harmonics are not considered. As long as the input voltage is a clean, single-frequency sinusoid, acceptable performance results.

4.3. Application of an EKF to Sensorless PFC

A PFC converter has two goals: voltage regulation and current tracking. To satisfy the downstream load, the output voltage must be a tightly regulated, nearly dc quantity. To achieve PFC, the input current must track a certain waveshape, usually a sinusoid whose frequency and phase match the input voltage. Often, two control loops are used to meet these two disparate goals. The voltage loop generates a current scale factor, then the current loop scales the sinusoidal waveform and forces input current to track the reference.

PFC is required by regulatory bodies [128] and minimizes input current for a given output power. The latter attribute can either be used to minimize wiring losses or to maximize output power. Interesting applications range from tens of watts to a few kilowatts. The power range can be broken into three smaller ranges:

- There are converter topologies for which average input current inherently tracks input voltage. Most operate in discontinuous conduction mode. Losses are higher than continuous conduction mode designs due to high

peak currents. However, below 100-W output, the total losses are small enough that the thermal management is straightforward. The low cost of the control circuit outweighs any additional expense in the components.

- Above 1 kW, the dollar value of the converter justifies fairly sophisticated controls. Hall effect current sensors are common. Giant magnetoresistive (GMR) current sensors are available. Existing digital control methods produce excellent performance.
- Between 100 W and 1 kW, neither extreme solution is applicable. Shunts are typically used for current sensing. Analog controllers are commonly used, although closed-loop performance over a wide operating range may require complicated feedback networks.

For the last category, a new current-sensorless control architecture would be attractive. Shunts are lossy and provide small, noisy signals. A Kalman filter could be used to improve sensor quality. However, given the added controller complexity inherent to a Kalman filter, a designer would like to eliminate something in exchange for adding a microprocessor.

This section presents a new current-sensorless PFC control algorithm that only uses voltages (input and output). Computational complexity is manageable with a DSP. High power factor (0.985) and low THD (9.3%) are achieved. The power circuit is a boost converter, as shown in Fig. 3.1.

4.3.1. Overview of control architecture

The controller is partitioned into a real power loop and a power factor angle loop. The real power affects the moving-average output voltage. Unity power factor

corresponds to a power factor angle of zero, so the power factor angle can be used to control input current. The overall system diagram is shown in Fig. 4.3. The individual blocks will be discussed throughout the following subsections.

Real power can be considered in the phasor domain. For a sufficiently high switching frequency, the boost converter of Fig. 3.1 can be modeled as a rectified ac voltage source with rms magnitude V_{eq} and phase angle $\psi + \theta$ connected to the line through an impedance $j\omega L = jX_L$. That is, the angle between \bar{V}_{eq} and \bar{V}_{in} (in the phasor domain) is ψ . The real power into the converter is

$$P_{in} = -\frac{V_{inrms}V_{eq}}{X_L}\sin\psi \approx -\frac{V_{pk}^2}{2X_L}\psi \quad (4.14)$$

The magnitude V_{eq} is adjusted to maintain near-zero reactive power, so

$$V_{eq} \approx V_{inrms} = \frac{V_{pk}}{\sqrt{2}}. \text{ Just as for a synchronous generator, the primary adjustment for real}$$

power is the phase angle ψ , which is small. Real power flow determines the change in output voltage, since any difference between input power P_{in} and load power P_{out} will charge or discharge the output capacitor C . The voltage across the capacitor can be partitioned into a slow-changing dc value V_{odc} plus a zero-mean ripple voltage at twice the line frequency. Power balance only affects V_{odc} .

The nonlinear capacitor voltage dynamics of a boost converter can be linearized through a change of coordinates. Instead of V_{odc} as a state, the stored energy

$$E = \frac{1}{2}CV_{odc}^2 \quad (4.15)$$

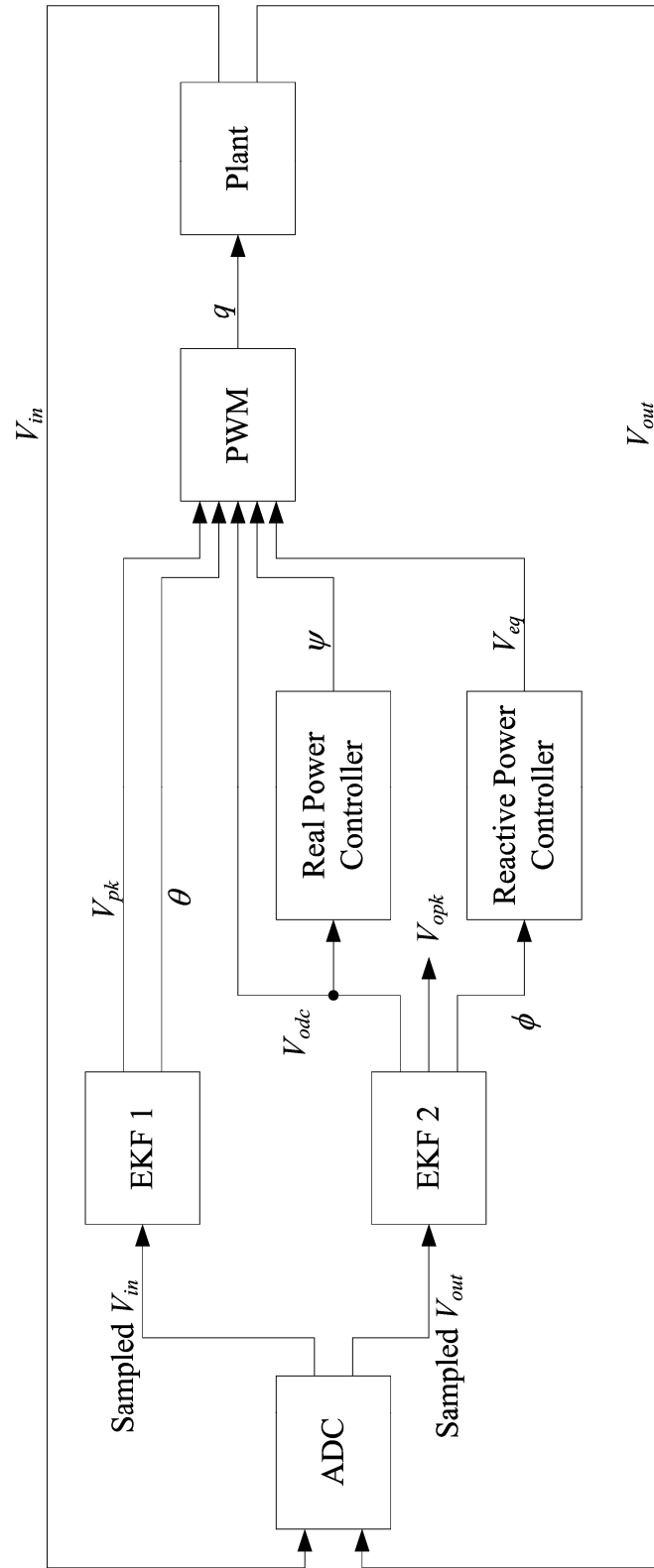


Fig. 4.3. Block diagram of sensorless PFC algorithm.

is used [73, 123]. The discrete-time dynamical equation for E is linear with a sample rate of $T_{ripple} = \frac{1}{120}$ s.

$$E[k] = E[k-1] + (P_{in} - P_{out})T_{ripple} \quad (4.16)$$

Linear discrete-time systems can achieve deadbeat performance. The control law is

$$\begin{aligned} \psi[k+1] &= \psi[k] + \frac{1}{G}(E_{ref} - 2E[k] + E[k-1]) \\ G &= -\frac{V_{pk}^2}{2\omega L} \end{aligned} \quad (4.17)$$

E_{ref} is the reference energy, i.e., the value of E at the reference output voltage. True deadbeat performance can be achieved if there is no sensing delay and if an accurate value of V_{pk} is used to compute G . Adequate performance is achieved if V_{odc} is the output of a Kalman filter and if an approximately correct value of V_{pk} (e.g., 170 V) is used to compute G .

The other control objective is to force current to follow a sinusoidal reference, or equivalently, to force the power factor angle to zero. The ripple portion of the capacitor voltage is

$$V_{oripple} = V_{opk} \sin(2\omega t + \phi + \theta) \quad (4.18)$$

Again, θ is the offset determined from sensed line voltage zero crossing. If ϕ can be somehow estimated, a controller can drive ϕ to zero and achieve unity power factor. A reasonable control law is a simple discrete-time PI controller,

$$\begin{aligned} V_{eq}[k] &= V_{inrms}[k] + K_p e_\phi[k] + K_I e_I[k] \\ e_\phi[k] &= \phi_{ref} - \phi[k] \\ e_I[k] &= e_I[k-1] + e_\phi[k] \end{aligned} \quad (4.19)$$

The same sample rate, T_{ripple} , applies as for the real power loop. For unity power factor, $\phi_{ref} = 0$.

The basic architecture uses two control loops to regulate two portions of the output (capacitor) voltage. Real power regulates the slow-changing dc value. Reactive power regulates the power factor angle. Both loops depend on partitioned knowledge of output voltage, which can be obtained with an EKF.

4.3.2. EKF for voltage sensing

The controller needs knowledge of dc and ac portions of the output voltage. As in the input voltage sensing algorithm of Section 4.2, the output voltage can be represented by a fictitious dynamical system.

$$\begin{bmatrix} V_{opk} \\ \phi \\ V_{odc} \end{bmatrix} [k] = \begin{bmatrix} V_{opk} \\ \phi \\ V_{odc} \end{bmatrix} [k-1] + \mathbf{w}_o [k-1] \quad (4.20)$$

$$V_o [k] = V_{opk} [k] \sin(2k\omega T + \phi[k] + \theta[k]) + V_{odc} [k] + v_o [k]$$

The index k in (4.20) is updated every T , equal to the switching period. The sensing noise v_o is similar to v in (4.9), so similar variance applies. The random dynamics \mathbf{w}_o are affected both by the control laws ((4.17) and (4.19)) and by external factors such as load changes. The covariance matrix is

$$\mathbf{Q}_{V_o} = \begin{bmatrix} \sigma_{V_{opk}}^2 & m_{2V_{opk}\phi} & m_{2V_{opk}V_{odc}} \\ m_{2V_{opk}\phi} & \sigma_{\phi}^2 & m_{2\phi V_{odc}} \\ m_{2V_{opk}V_{odc}} & m_{2\phi V_{odc}} & \sigma_{V_{odc}}^2 \end{bmatrix} \quad (4.21)$$

The variances on the main diagonal reflect changes in just one aspect of the output voltage. The covariance terms (second moments) on the off-diagonals reflect interactions between the different aspects.

Appropriate values for \mathbf{Q}_{V_0} can be estimated from limits on system transients.

The magnitude of the ripple voltage depends on the load power and the bus capacitance.

Suppose the rated output current is I_{dc} and the nominal bus voltage is V_{bus} . The maximum possible output power is $I_{dc}V_{bus}$. The peak of the power ripple in the capacitor is equal to the output power, at unity power factor. The ripple current, which is at twice the line frequency, has a peak amplitude

$$I_{acpk} = V_{opk} \times 2\omega C \quad (4.22)$$

So at maximum power,

$$V_{bus} V_{opk} \times 2\omega C = I_{dc} V_{bus} \quad (4.23)$$

Solving for V_{opk} , we find

$$V_{opk} = \frac{I_{dc}}{2\omega C} \quad (4.24)$$

Without limiting the generality of the method, the load power could change from its minimum value (zero) to its maximum value ($I_{dc}V_{bus}$) in one zero-crossing period T_{ripple} .

Typically, the changes will be much smaller. So \mathbf{w}_{o1} can be approximated as a Gaussian random variable with zero mean and standard deviation

$$\sigma_{V_{opk}} = \frac{1}{3} \frac{I_{dc}}{2\omega C} \frac{T}{T_{ripple}} \quad (4.25)$$

The factor of 1/3 means that a 3σ event is the maximum possible change. The last factor scales the change from the zero-crossing period to the sampling period, so that the Kalman filter may be updated more often. The standard deviation of (4.25) can be simplified further with

$$\omega = \frac{\pi}{T_{ripple}} \quad (4.26)$$

The variance needed for \mathbf{Q}_{Vo11} is

$$\sigma_{V_{opk}}^2 = \left(\frac{I_{dc} T}{6\pi C} \right)^2 \quad (4.27)$$

Similar analysis applies to the other diagonal terms. Given some ϕ_{\max} (typically about 0.1 rad, if the controller is operating properly),

$$\sigma_{\phi}^2 = \left(\frac{\phi_{\max} T}{3T_{\text{ripple}}} \right)^2 \quad (4.28)$$

Power balance in the capacitor gives

$$\sigma_{V_{odc}}^2 = \left(\frac{I_{dc} T}{3C} \right)^2 \quad (4.29)$$

With basic knowledge of operational limits, the main diagonals of \mathbf{Q}_{Vo} are approximated.

The covariance terms, the off-diagonal elements of \mathbf{Q}_{Vo} , are poorly defined, as they depend on the operational scenario. For example, for a step increase in load current, V_{odc} will decrease and V_{opk} will increase; ϕ may or may not change. If the controller causes the power factor angle to shift from lagging towards unity, ϕ will decrease and V_{opk} will decrease; V_{odc} may or may not change. If the controller causes a positive power imbalance, V_{odc} will increase and V_{opk} will increase; ϕ may or may not change. Many more scenarios are possible with unknown effects on the three variables.

The covariances are related to the variances, that is,

$$m_{2V_{odc}V_{opk}} \propto \sigma_{V_{odc}} \sigma_{V_{opk}} \quad (4.30)$$

and so forth. The constant of proportionality depends on the dynamics of the system and the external disturbances, and must fall within the interval [-1,1]. Since the external

factors are unknown, nearly any proportionality is defensible. The experimental system used

$$\mathbf{Q}_{Vo} = \begin{bmatrix} \sigma_{Vopk}^2 & 0.1\sigma_{Vopk}\sigma_{\phi} & -0.1\sigma_{Vopk}\sigma_{Vodc} \\ 0.1\sigma_{Vopk}\sigma_{\phi} & \sigma_{\phi}^2 & 0.1\sigma_{Vodc}\sigma_{\phi} \\ -0.1\sigma_{Vopk}\sigma_{Vodc} & 0.1\sigma_{Vodc}\sigma_{\phi} & \sigma_{Vodc}^2 \end{bmatrix} \quad (4.31)$$

These values gave the best overall experimental performance. See Sections 4.3.4 and 4.4 below for discussion and sensitivity analysis.

The complete control system is shown above in Fig. 4.3. EKF1 is based on (4.9)-(4.13). EKF2 is based on (4.20)-(4.31). The real power controller, which regulates output voltage, is given by (4.17). The reactive power controller, which ensures unity power factor, is given by (4.19). The PWM block divides the instantaneous output voltage command by the bus voltage to find duty cycle. The DSP has a hardware PWM module that creates the switching waveform q from the duty cycle command. The plant is the boost converter plus interface circuits. Setup code (a MATLAB script) is given in Appendix D. Simulink code is given in Appendix E.

4.3.3. Experimental sensorless PFC

The control algorithm and EKF are both built on many assumptions about input voltage, load type, and converter dynamics. First a simulation was constructed to verify proper control. As expected, the simulation worked well. However, a simulation cannot adequately capture the randomness of the physical system. That is, the simulation can include modeled random processes, but the models may not be accurate.

An experimental boost PFC converter was built to verify the model accuracy and control effectiveness. The basic framework relied on the modular inverter previously built by a team of graduate students [191]. The front-end active rectifier in the original

modular inverter was designed for three-phase 208 V, so a new front-end section was built with hardware appropriate for single-phase PFC. The schematic for the new printed circuit board, PCB50006 revision A, is shown in Appendix B. Power components are listed in Table 4.1. The nominal output rating is 6 A (1140 W). Several tests were performed with resistive loads.

The boost converter meets the requirement for time-scale separation. The characteristic impedance is $\sqrt{\frac{L}{C}} = 1.37 \Omega$. The nominal parasitic resistance R_L is 1.33Ω .

While the converter does not meet the conservative bound of (3.19), the requirement of (3.17) is satisfied for all values of u between 0 and 1. Figure 4.4 shows the left-hand side (LHS) and right-hand side (RHS) of (3.17) for the parameter values of Table 4.1. So long as the RHS always exceeds the LHS, time-scale separation is assured.

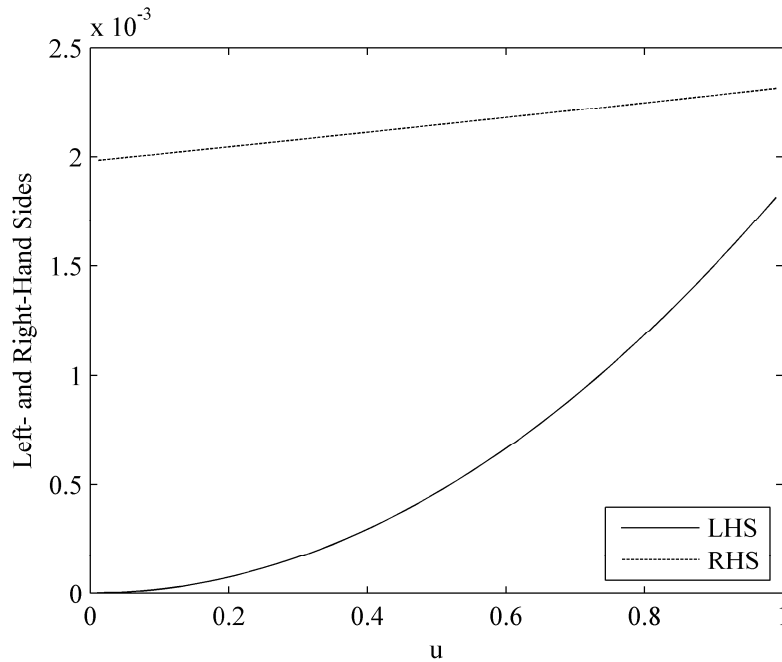


Fig. 4.4. Left-hand and right-hand side values of Eq. (3.17) for the parameters of Table 4.1.

TABLE 4.1. EXPERIMENTAL CONVERTER PARAMETERS.

Main Switch	STW20NK50
Fast Diode	HFA25PB60
Inductance	3 mH
Capacitance	1800 μ F
Parasitic Resistance R_L	1.33 Ω
Capacitor Resistance R_C	0.11 Ω
Input Voltage (Nominal)	120 V
Output Voltage	190 V
Switching Frequency	25 kHz

In general, performance improved with increased load. At light loads (below 0.5 A), the bus voltage ripple was too small to be reliably detected. The converter oscillated between relatively large, sinusoidal currents and zero current due to overvoltage. At moderate loads, the system performed as expected although some oscillation was observed in the magnitude of the line current. Figures 4.5-4.6 show experimental performance with a 100 Ω (1.9 A or 361 W) load. Figure 4.7 shows the harmonic spectrum of the line current, from a fast Fourier transform of the sampled data in Fig. 4.5. The total power factor is 0.985. The total harmonic distortion (THD) is 10.6%.

The Kalman filters were constructed with the covariance matrices described in Section 4.3.2. The deadbeat voltage control gain of (4.17) was used, with an approximate value of 170 V substituted for the real (sensed) V_{pk} . In the PI controller of (4.19), $K_p = 10$ and $K_i = 0.2083$. Larger gains produced unacceptable oscillatory behavior.

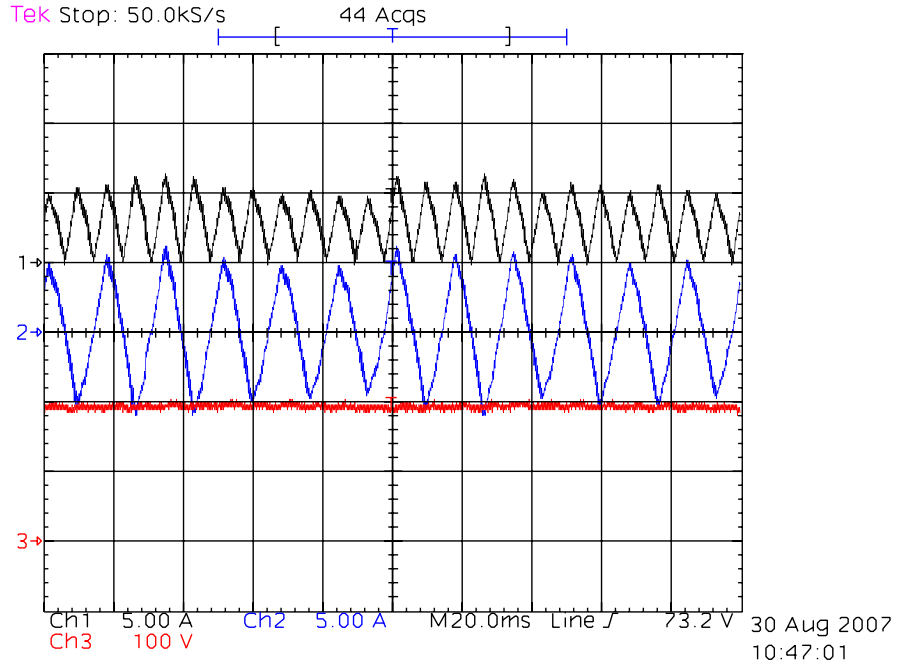


Fig. 4.5. Experimental sensorless PFC. top waveform, channel 1, inductor current, 5 A/div; middle waveform, channel 2, line current, 5 A/div; bottom waveform, channel 3, bus voltage, 100 V/div; horizontal scale 20 ms/div.

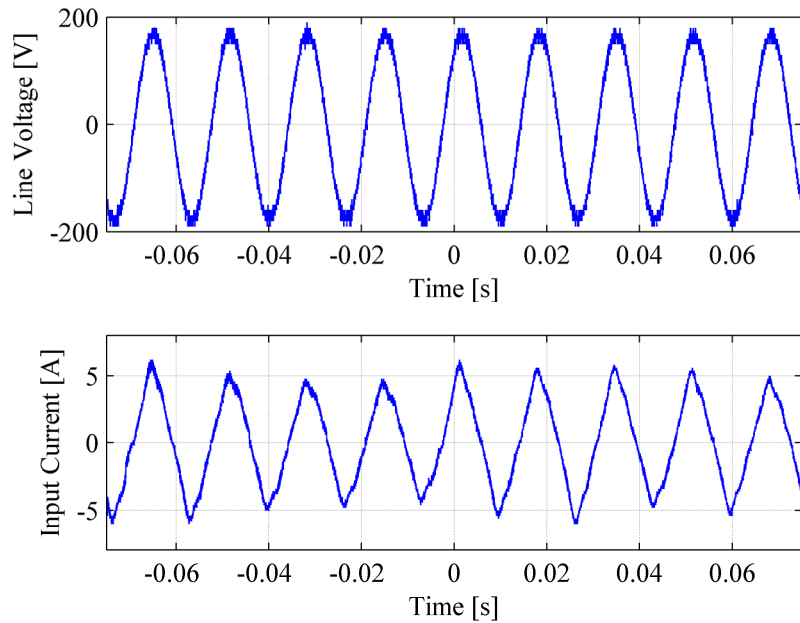


Fig. 4.6. As in Fig. 4.5, with line voltage also shown.

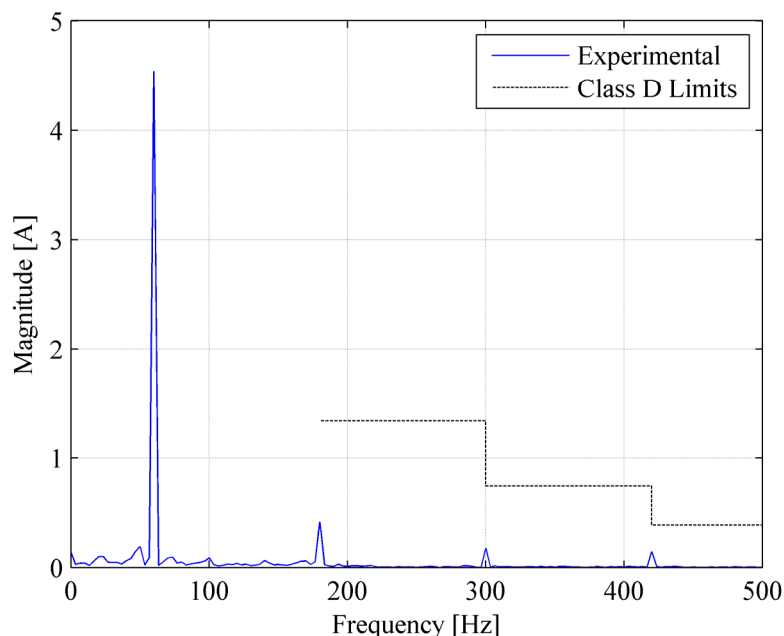


Fig. 4.7. Harmonic spectrum (FFT) of line current from Fig. 4.5 with IEC limits.

The oscillation evident in Figs. 4.5-4.6 results from residual sensed noise. The Kalman filter attenuates, rather than eliminates, quantization effects. The voltage control loop has high gain, so the residual noise causes random fluctuations in the line current magnitude. The designer must trade this oscillatory behavior against the need for fast transient response. PFC voltage loop stability was the topic of [192], though much of that work used continuous-time concepts and assumed a time scale faster than T_{ripple} .

PFC serves two purposes: it minimizes rms line current for a given output power, and it allows a device to meet regulatory requirements such as [128]. With a power factor of 0.985, the line current will exceed the ideal unity power factor line current by 1.6%. The harmonic currents shown in Fig. 4.7 are far below the regulatory limits. The most stringent requirements in [128] are for class D equipment, which includes computers. While other classes of equipment must meet absolute harmonic current limits, class D equipment must meet relative limits shown in Table 4.2 (from Table 3 in [128]).

Table 4.2 also shows the harmonic performance of the experimental system, which is at least a factor of three better than the requirements. Figure 4.7 also shows the limits superimposed on the FFT. The limits only apply to the first 39 harmonics, or 2340 Hz. Since the switching frequency is 25 kHz, switching harmonics do not affect compliance. Overall, the experimental system far exceeds regulatory requirements and requires only 1.6% more current than a system with true unity power factor.

4.3.4. Sensitivity to parameters and conditions

A sensitivity study was performed to determine the effect of Q_{Vo} on system performance. As discussed above, the value of Q_{Vo} is somewhat unknown. Figure 4.8 shows six variations. Figures 4.8(a)-(c) use the base value for Q_{Vo} while the load varies. Figures 4.8(d)-(f) use different values for the off-diagonal entries in Q_{Vo} . The variations are summarized in Table 4.3. Over all parameter values and operating conditions, THD never exceeded 15% and power factor always exceed 0.97. In general, lower current corresponds to lower THD and lower power factor. Values of Q_{Vo} do not materially affect THD or power factor.

TABLE 4.2. IEC 61000-3-2 CLASS D LIMITS ON HARMONIC CURRENTS.

Harmonic order n	Maximum permissible harmonic current per watt (mA/W)	Maximum permissible harmonic current (A)	Limit at Experimental 393 W input (A)	Experimental Harmonic Current (A)
3	3.4	2.30	1.337	0.423
5	1.9	1.14	0.747	0.174
7	1.0	0.77	0.393	0.145
9	0.5	0.40	0.197	0.024
11	0.35	0.33	0.138	0.007
13	0.30	0.21	0.117	0.001
$15 \leq n \leq 39$	$3.85/n$	$2.25/n$	$1.513/n$	smaller

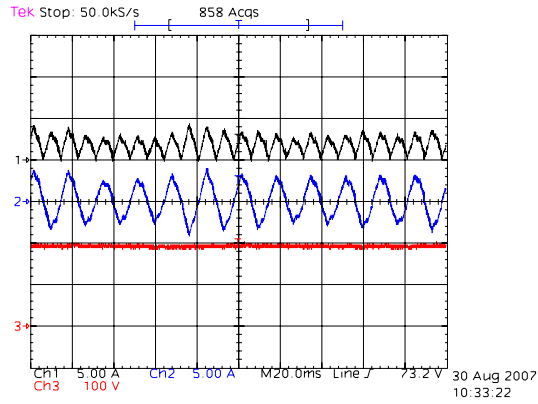
TABLE 4.3. SENSITIVITY STUDY PARAMETERS AND CONDITIONS.

Figure	Q_{Vo}	Load Current [A]
4.3(a)	$\begin{bmatrix} \sigma_{Vopk}^2 & 0.1\sigma_{Vopk}\sigma_\phi & -0.1\sigma_{Vopk}\sigma_{Vodc} \\ 0.1\sigma_{Vopk}\sigma_\phi & \sigma_\phi^2 & 0.1\sigma_{Vodc}\sigma_\phi \\ -0.1\sigma_{Vopk}\sigma_{Vodc} & 0.1\sigma_{Vodc}\sigma_\phi & \sigma_{Vodc}^2 \end{bmatrix}$ (base)	1.14
4.3(b)	Base	2.66
4.3(c)	Base	Step from 1.14 to 2.66
4.3(d)	$\begin{bmatrix} \sigma_{Vopk}^2 & 0.1\sigma_{Vopk}\sigma_\phi & 0.3\sigma_{Vopk}\sigma_{Vodc} \\ 0.1\sigma_{Vopk}\sigma_\phi & \sigma_\phi^2 & 0.1\sigma_{Vodc}\sigma_\phi \\ 0.3\sigma_{Vopk}\sigma_{Vodc} & 0.1\sigma_{Vodc}\sigma_\phi & \sigma_{Vodc}^2 \end{bmatrix}$	1.90
4.3(e)	$\begin{bmatrix} \sigma_{Vopk}^2 & -0.1\sigma_{Vopk}\sigma_\phi & -0.1\sigma_{Vopk}\sigma_{Vodc} \\ -0.1\sigma_{Vopk}\sigma_\phi & \sigma_\phi^2 & 0.1\sigma_{Vodc}\sigma_\phi \\ -0.1\sigma_{Vopk}\sigma_{Vodc} & 0.1\sigma_{Vodc}\sigma_\phi & \sigma_{Vodc}^2 \end{bmatrix}$	1.90
4.3(f)	$\begin{bmatrix} \sigma_{Vopk}^2 & 0.1\sigma_{Vopk}\sigma_\phi & -0.1\sigma_{Vopk}\sigma_{Vodc} \\ 0.1\sigma_{Vopk}\sigma_\phi & \sigma_\phi^2 & -0.1\sigma_{Vodc}\sigma_\phi \\ -0.1\sigma_{Vopk}\sigma_{Vodc} & -0.1\sigma_{Vodc}\sigma_\phi & \sigma_{Vodc}^2 \end{bmatrix}$	1.90

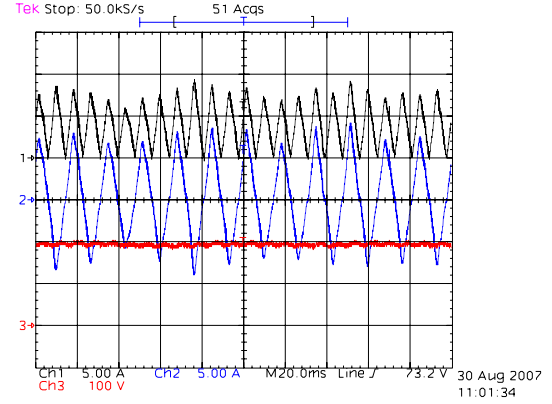
4.4. Summary

This chapter presented Kalman filters and EKF's for switching power converters. A Kalman filter estimates state variables in a stochastic system. The additive random variables may affect both sensing and dynamics. An EKF includes nonlinearities in the plant or output equation.

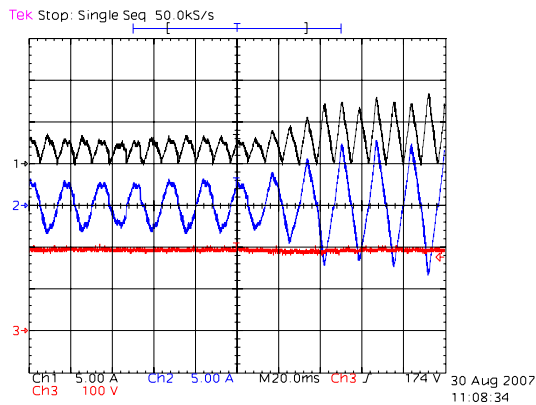
Conventional notions of “states” must be reexamined in the stochastic context. Two examples were shown, neither of which used capacitor voltages or inductor currents as states. Rather, the example EKF's used waveform parameters to extract useful information about system operation. A useful perspective is to treat EKF's as signal processing elements, not control elements.



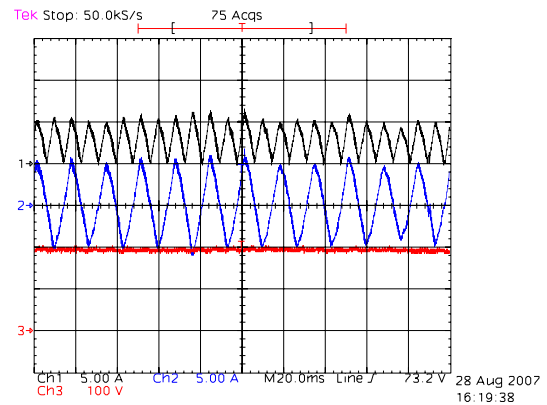
(a)



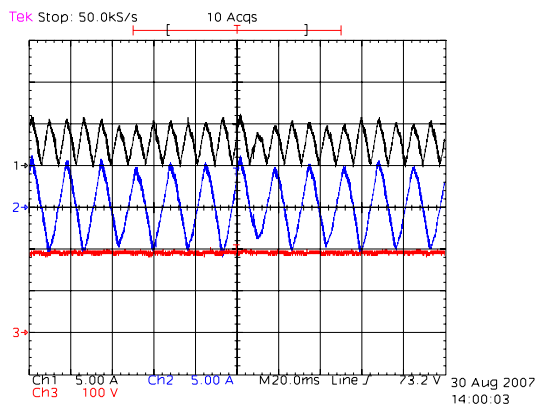
(b)



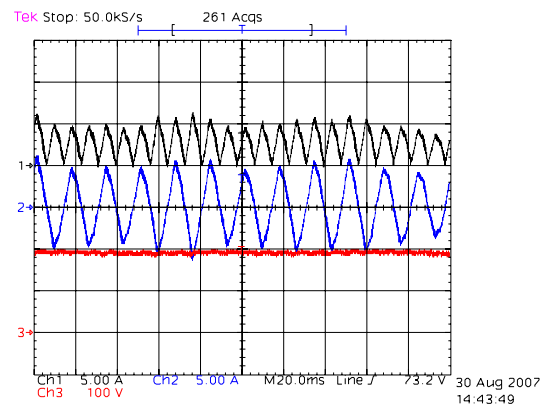
(c)



(d)



(e)



(f)

Fig. 4.8. Sensitivity study waveforms for experimental PFC. All oscillograms use identical settings. Top waveforms, channel 1, inductor current, 5 A/div; middle waveforms, channel 2, line current, 5 A/div; bottom waveforms, channel 3, bus voltage, 100 V/div; horizontal scale 20 ms/div. The cases (a)-(f) are described in Table 4.3.

A current-sensorless PFC algorithm was demonstrated. The control architecture used EKFs to determine appropriate waveform parameters. Then, the control objectives were cast in the phasor domain and separated into real and reactive power loops. The real power loop can theoretically achieve deadbeat performance, although the inherent delay of the EKF causes some oscillation. The reactive power loop forces the line current to be nearly sinusoidal. The power factor is high, 0.985, while the THD is low, 10.6%.

Instead of stochastic assumptions, a designer could perform worst-case analysis. While such an approach can provide useful stability results, the objective of a PFC converter is reference tracking, not equilibrium stability. The worst-case error can be substantial, and a boost converter has high voltage-to-current gain. Suppose, for example, that the worst-case timing error of $\theta = \omega T$ is assumed. The power error would be 193 W in the experimental converter, which is 17% of the system rating. So, a worst-case analysis would result in excessive system oscillations that may or may not be adequately attenuated by feedback.

Kalman filters and EKFs have huge potential in power electronics applications. A first application, current-sensorless PFC, has the potential to impact ac-dc converters with moderate-to-high power ratings. Other potential applications include line impedance monitoring, load estimation, and detection of undesirable converter interactions.

CHAPTER 5

DISCRETE-TIME RIPPLE CORRELATION CONTROL

DRCC is an application of digital control that demonstrates the use of synchronized sampling to obtain information about the operating point. This contrasts to the work in the previous chapter, which used Kalman filters to mitigate the loss of information that results from asynchronous sampling.

RCC is an online optimization method particularly suited for switching power converters. Its objective is to maximize or minimize a cost function, usually a power or energy quantity. RCC uses information present in the inherent switching ripple to determine the gradient of the cost function. The result is that information available on the fast time scale (current and voltage ripple) enables the control to attain a slow time scale objective (operation at the optimum). RCC is well-established in a continuous-time framework [30, 134-138, 144-149, 167-169].

DRCC extends RCC to the discrete-time domain [193]. A brief summary of RCC is included in Section 5.1 for background. In principle, the RCC signals could be sampled at a high rate and the continuous-time method could be transformed to discrete-time. In practice, though, knowledge of waveshapes can be used to drastically reduce the sampling requirement while achieving equivalent results, as shown in Section 5.2. Section 5.3 contains a stability proof, and Section 5.4 describes an experimental version.

5.1. Ripple Correlation Control

RCC uses switching ripple to optimize a cost function J that is solely a function of a state variable z . The experimental converter described in Section 5.4 is an MPPT for a photovoltaic panel, so the development in Sections 5.1 through 5.3 will assume that the

objective is to maximize J . An equivalent formulation can be developed to minimize a cost function, as in efficiency maximization (power minimization), with a sign change. Global stability requires that J is unimodal, that is, there is a single global extremum.

For a suitable cost function $J(z)$, the maximum value occurs where

$$\frac{dJ}{dz} = 0 \quad (5.1)$$

The power conversion plant has an input u . Just as J must be unimodal, the steady state value

$$\varphi(u) = \lim_{t \rightarrow \infty} z(u, t) \quad (5.2)$$

must be monotonic over the operating range. An integral control law

$$u = k \int \frac{dJ}{dz} dt \quad (5.3)$$

will drive the operating point to the maximum value of J . The sign of k and the effect of u on z determine whether the control law goes towards a maximum or a minimum. The magnitude of k influences convergence rate.

Usually, derivatives like (dJ/dz) are unavailable in a practical system, so a better controller is needed. If the integrand of (5.3) is multiplied by a positive value, the

equilibrium operating point does not change. A convenient multiplier is $\left(\frac{dz}{dt}\right)^2$, which

yields

$$u = k \int \frac{dJ}{dz} \frac{dz}{dt} \frac{dz}{dt} dt = k \int \frac{dJ}{dt} \frac{dz}{dt} dt \quad (5.4)$$

Now the control law only needs time derivatives. This transformation is possible if (dz/dt) is nonzero, except perhaps at isolated points. If the converter is always switching with duty cycle $D \in (0,1)$, then the derivative of z is nonzero except at switching edges.

Many approximations to (5.4) have been suggested, all of which require at least one multiplication. Often, (dz/dt) is piecewise constant. If the sign information is adequate, then a synchronous demodulator can be used. In this approach, J is calculated (usually with a multiplication), (dJ/dt) is determined with a filter, $(-dJ/dt)$ is determined with an inverting amplifier, and analog switches controlled by $\text{sgn}(dz/dt)$ determine the integrand of (5.4). This approach was used in [167, 168]. Another variation is to consider only the phase information [169, 194]. In this formulation, RCC resembles a phase-locked loop. In principle, the two simplifications can be combined, where the integrand is approximated as $\text{sgn}(dJ/dt)\text{sgn}(dz/dt)$. These approximations affect noise immunity, convergence rate, and potentially the equilibrium value.

RCC is typically implemented with analog circuits. Time derivatives can be obtained easily. To achieve better noise immunity, though, the “derivative” stage is usually a filter whose gain rolls off somewhere above the switching frequency. Multiplication is possible with an analog multiplier such as an AD633. Unfortunately, a typical analog multiplier is power-hungry: an AD633 consumes 4 mA at ± 15 V, or 120 mW.

RCC is a generic online optimization technique. As long as states and cost functions that both contain ripple can be identified, there will be adequate information to find the optimum operating point. RCC is particularly well-suited to switching power

converters, since the switching action continuously perturbs the states and creates the necessary ripple. RCC has also been proposed for motor drive applications. The stored energy in the motor's magnetic field may damp out the ripple that results from the main switching elements. In this case, an extra ripple term at a suitably low frequency can be added to obtain the necessary information. Other observer-based solutions are likely possible.

RCC is conceptually related to vibrational control [195]. Vibrational control is concerned with systems that have uncontrollable unstable modes. Under certain conditions, stability can be obtained if the plant dynamics are changed from

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} \quad (5.5)$$

to

$$\dot{\mathbf{x}} = (\mathbf{A} + \mathbf{B}(t))\mathbf{x} \quad (5.6)$$

The new term, $\mathbf{B}(t)$, varies periodically and has zero mean. The combined dynamics can be designed to be stable. In RCC, the original system (usually a switching power converter) has inherent periodic variation, as discussed in Chapter 3. The inherent ripple produces information that can be used to achieve a particular control goal, optimization of an energy function.

5.2. Discrete-Time Formulation

A digital version of RCC is preferable for many reasons. While analog multipliers are power-hungry, low-power microcontrollers are available with hardware digital multipliers. For example, an MSP430F148 has a hardware 8x8 bit multiplier, and the total microprocessor core consumes less than 1 mA at 2.5 V (2.5 mW). A digital implementation enables other features, too, such as protection modes and user interface.

The analog control law (5.4) could be converted to discrete-time with fast sampling, e.g., 10 or more samples per switching period with a suitable high-end microcontroller or DSP.

The application of some waveform knowledge yields a simpler control law. In most cases, z is piecewise linear, so its time derivative is piecewise constant.

$$\dot{z} = \begin{cases} w_+ & \text{mod}(t, T) \in [0, DT) \\ w_- & \text{mod}(t, T) \in [DT, T) \end{cases} \quad (5.7)$$

T is the switching period. D is the fraction of the period when $\dot{z} > 0$, which may or may not be the same as the duty cycle of a controlled switch. Both D and T may vary, so long as neither goes to zero and D does not go to 1. This form for \dot{z} can be substituted into (5.4). A definite integral determines the change in u over a single period. The period can be subdivided according to the value of \dot{z} and the definite integral can be evaluated symbolically.

$$\begin{aligned} u(T) &= u(0) + kw_+ \int_0^{DT} J dt + kw_- \int_{DT}^T J dt \\ u(T) &= u(0) + kw_+ (J(DT) - J(0)) + kw_- (J(T) - J(DT)) \end{aligned} \quad (5.8)$$

This result (5.8) can be generalized to any switching period that is aligned with the minimum of z (the rising edge of \dot{z}). In periodic steady-state,

$$\begin{aligned} J(0) &= J(T) \\ w_+ D + w_- (1 - D) &= 0 \end{aligned} \quad (5.9)$$

These relationships (5.9) can be substituted into (5.8) to give a final control law of

$$u(T) = u(0) + \frac{kw_+}{1-D} (J(DT) - J(0)) \quad (5.10)$$

Just as many approximations have been proposed for the analog RCC law (5.4), there is a good simplification for (5.10). Instead of using a gain on the difference between samples

of J , use a gain on the *sign* of the difference. If the actuation is quantized coarsely, there may be no practical difference between (5.10) and

$$u(T) = u(0) + \hat{k} \operatorname{sgn}(J(DT) - J(0)) \quad (5.11)$$

This control law is related to delta modulation [107]. To generalize, the input need not be updated every cycle. For example, the experimental system discussed below uses a controller of the form

$$u(t_0 + nT) = u(t_0) + \hat{k} \operatorname{sgn}(J(t_0 + (n-1+D)T) - J(t_0 + (n-1)T)) \quad (5.12)$$

All of the needed information on the operating point can be obtained from two samples taken at appropriate times, when the state variable is at a maximum or minimum. At equilibrium, J oscillates around the maximum at twice the switching frequency and reaches the same value at each end of the oscillation. The sampling process is shown in Figs. 5.1 and 5.2 for a MPPT. The generic cost function J is implemented as p , the panel power. The state variable z is chosen as i , the panel current. Panel voltage v is also sampled to compute $p = vi$. In Fig. 5.1, the panel is not at the maximum power point (current needs to increase). In Fig. 5.2, the panel is at the maximum power point. The power passes through the maximum twice in each switching cycle, once while the current is increasing and once while the current is decreasing.

Although the DRCC control law resembles the perturb-and-observe (P&O) method [196], there are two primary differences. First, the time scale is far different. The P&O technique uses two samples of output power that correspond to two steady-state operating points. DRCC uses a pair of samples within a single switching period. While the stability proof given below for DRCC assumes pairs are separate enough that the system is near steady-state, a practical application may sample more frequently. The

update rate can be as fast as the switching frequency. Second, P&O always leaves the present operating point to determine if the optimum is nearby. DRCC, though, uses information in the ripple at the present operating point to determine if equilibrium has been reached. P&O always exhibits subharmonics (at a fraction of the update rate), while DRCC can achieve true equilibrium.

5.3. DRCC Stability

Although the stability of continuous-time RCC was proven in [144], a new stability proof is needed for DRCC. There are two aspects to prove: first, that the equilibrium corresponds to the optimum, and second, that the control law (5.12) will cause the operating point to converge to the equilibrium. The proof will consider only the maximization problem, since minimization can be achieved with a simple sign change.

A few assumptions and definitions are necessary. The plant has an average model

$$\frac{dz}{dt} = f(z, u) \quad (5.13)$$

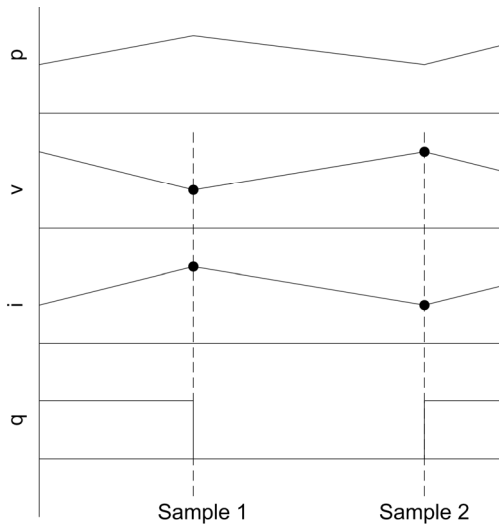


Fig. 5.1. Sample timing away from maximum power point (current is too low). Waveforms are switching function q , panel voltage v , current i , and power p .

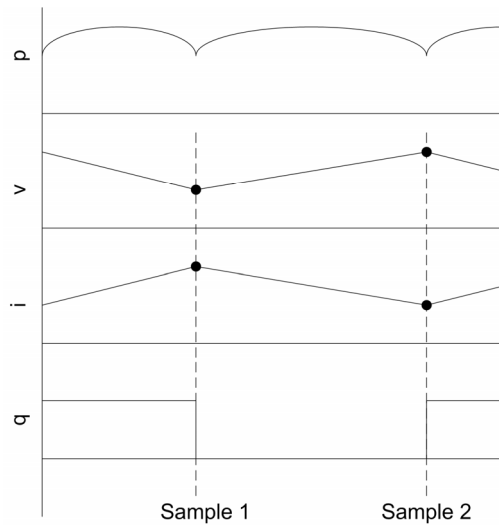


Fig. 5.2. Sample timing at the maximum power point. Waveforms are switching function q , panel voltage v , current i , and power p .

The average-model state variable z can be related to the physical state variable x with an algebraic ripple correction term ψ ,

$$x(t) = z(t) + \psi(u, t) \quad (5.14)$$

Although the variable names and terminology are different, this is the same concept as in KBM averaging (see Section 3.3.2). The ripple ψ is small (relative to x and z) with zero mean over a switching period. The dynamical system (5.13) has an equilibrium at $z = \varphi(u)$. The input is constrained such that

$$u \in [u_{\min}, u_{\max}] \quad (5.15)$$

The equilibrium function $\varphi(u)$ is monotonic on this interval. The cost function $J(z)$ is unimodal, so there is a unique maximum

$$\max_{u \in [u_{\min}, u_{\max}]} J(\varphi(u)) = J(\varphi^*) = J^* \quad (5.16)$$

Equilibrium is reached where the control law (5.12) causes no change in u from sample to sample. The input u is updated every nT based on two samples of J during the immediately preceding switching interval. By the definition of duty cycle, the change in u is

$$\hat{k} \operatorname{sgn} \left(J \left(z + \min_{t \in [(n-1)T, nT]} \psi(u, t) \right) - J \left(z + \max_{t \in [(n-1)T, nT]} \psi(u, t) \right) \right) \quad (5.17)$$

If nT is sufficiently large, $z \approx \varphi(u)$. Rolle's theorem states, for generic functions:

Let f be continuous on the closed interval $[a, b]$ and differentiable on the open interval (a, b) . If $f(a) = f(b)$, then there is at least one number c in (a, b) such that $f'(c) = 0$.

This applies to DRCC directly. Equilibrium corresponds to a point where u no longer changes, which means that the two samples of J are equal. To restate Rolle's theorem in the appropriate variables,

Let J be continuous on the closed interval

$$\left[\varphi(u(t_0)) + \min_{t \in [(n-1)T, nT]} \psi(u(t_0), t), \varphi(u(t_0)) + \max_{t \in [(n-1)T, nT]} \psi(u(t_0), t) \right] \quad (5.18)$$

and differentiable on the corresponding open interval. If

$$J\left(\varphi(u(t_0)) + \min_{t \in [(n-1)T, nT]} \psi(u(t_0), t)\right) = J\left(\varphi(u(t_0)) + \max_{t \in [(n-1)T, nT]} \psi(u(t_0), t)\right) \quad (5.19)$$

then there is at least one number φ^* in the interval (5.18) such that

$$\frac{dJ}{dz}(\varphi^*) = 0 \quad (5.20)$$

So, the equilibrium occurs where the ripple band encloses the maximum. This is as close to the maximum as any sample-based control law can reach without full knowledge of the plant dynamics. The ripple band can be made arbitrarily small through design choices that trade tracking accuracy and signal-to-noise ratio.

Since the equilibrium is the correct operating point, the next objective is to prove that the control law (5.12) will converge to the equilibrium. Define

$$\begin{aligned} \Delta J &= J(\varphi(u(t_0 + nT))) - J(\varphi(u(t_0))) \\ \Delta \varphi &= \varphi(u(t_0 + nT)) - \varphi(u(t_0)) \\ \Delta u &= u(t_0 + nT) - u(t_0) \end{aligned} \quad (5.21)$$

The third new variable, Δu , is determined by (5.12). For sufficiently small Δu ,

$$\begin{aligned}\Delta J &= \Delta\varphi \times \frac{dJ}{d\varphi}(\varphi(u(t_0))) \\ \Delta\varphi &= \Delta u \times \frac{d\varphi}{du}(u(t_0))\end{aligned}\tag{5.22}$$

Two derivatives are needed in (5.22). For sufficiently small ripple,

$$\frac{dJ}{d\varphi}(\varphi(u(t_0))) \approx \frac{J\left(\varphi(u(t_0)) + \min_{t \in [(n-1)T, nT]} \psi(u, t)\right) - J\left(\varphi(u(t_0)) + \max_{t \in [(n-1)T, nT]} \psi(u, t)\right)}{\min_{t \in [(n-1)T, nT]} \psi(u, t) - \max_{t \in [(n-1)T, nT]} \psi(u, t)}\tag{5.23}$$

That is, the derivative is approximated by the difference in two samples of J divided by the difference in the corresponding values of x . The other derivative, $\frac{d\varphi}{du}$, is known to be of constant sign since $\varphi(u)$ is monotonic. Through a series of substitutions, we find

$$\Delta J = \hat{k} \left(\frac{d\varphi}{du}(u(t_0)) \right) \left| \frac{J\left(\varphi(u(t_0)) + \min_{t \in [(n-1)T, nT]} \psi(u, t)\right) - J\left(\varphi(u(t_0)) + \max_{t \in [(n-1)T, nT]} \psi(u, t)\right)}{\min_{t \in [(n-1)T, nT]} \psi(u, t) - \max_{t \in [(n-1)T, nT]} \psi(u, t)} \right|\tag{5.24}$$

There are four factors in (5.24). The derivative $\frac{d\varphi}{du}$ is of constant sign because of monotonicity. The absolute value in the numerator results from multiplying the actual difference by the sign of the difference. The denominator is always negative, as the difference between a minimum and a maximum. The gain \hat{k} is constant and can be chosen so that ΔJ is always positive (approaching the desired operating point) or zero (at equilibrium). The sign of the gain must be

$$\text{sgn } \hat{k} = -\text{sgn } \frac{d\varphi}{du} \quad (5.25)$$

The magnitude of the gain is chosen for a particular problem so that the system quickly approaches the maximum without undue overshoot. Conceptually, this is similar to Newton's method or, more precisely, the secant method. A large gain will cause oscillation around the maximum, while a small gain will slowly traverse J until reaching equilibrium.

5.4. Application to Solar Power

RCC has been explored in detail for photovoltaic maximum power point tracking [136-138, 141, 142]. The MPPT application motivated the present work. DRCC offers several advantages over RCC, particularly low power consumption due to digital implementation.

Photovoltaic panels deliver maximum power at a particular operating point that varies with insolation and temperature. A typical I-V characteristic for a solar cell is

$$i_{panel}(v_{panel}) = I_{SC} \left(1 - \exp\left(\frac{v_{panel}}{mV_T}\right) \right) \quad (5.26)$$

I_{SC} is the short-circuit current, which varies linearly with the insolation. V_T is the thermal voltage (kT/q) and m is a technology-dependent scale factor. The voltage on a PV panel scales with the number of cells connected in series, while the current is limited by the weakest cell (to a first approximation). Power, the product of current and voltage, has a well-defined maximum where current is a large fraction of I_{SC} and voltage is a large fraction of the open-circuit voltage V_{OC} . Panel current and power, as functions of voltage, are shown in Fig. 5.3 for the panel used in the experiments to follow. Notice that the

peak power occurs at a panel voltage of about 17 V, compared to an open-circuit voltage of about 20.5 V.

DRCC can be used as part of a highly effective MPPT. MPPTs are used to operate a PV panel as close to the maximum power point as reasonably possible [133]. For the generic cost function J , an MPPT uses panel power p_{panel} . For the correlation variable z , an MPPT can use either panel current i_{panel} or panel voltage v_{panel} . As shown in [136, 141], RCC performs much better if voltage is used rather than current. In essence, correlation with v_{panel} minimizes the influence of stored energy in the panel capacitance. The sections to follow will discuss an appropriate MPPT implementation that uses mode-switching and DRCC to achieve fast, robust tracking.

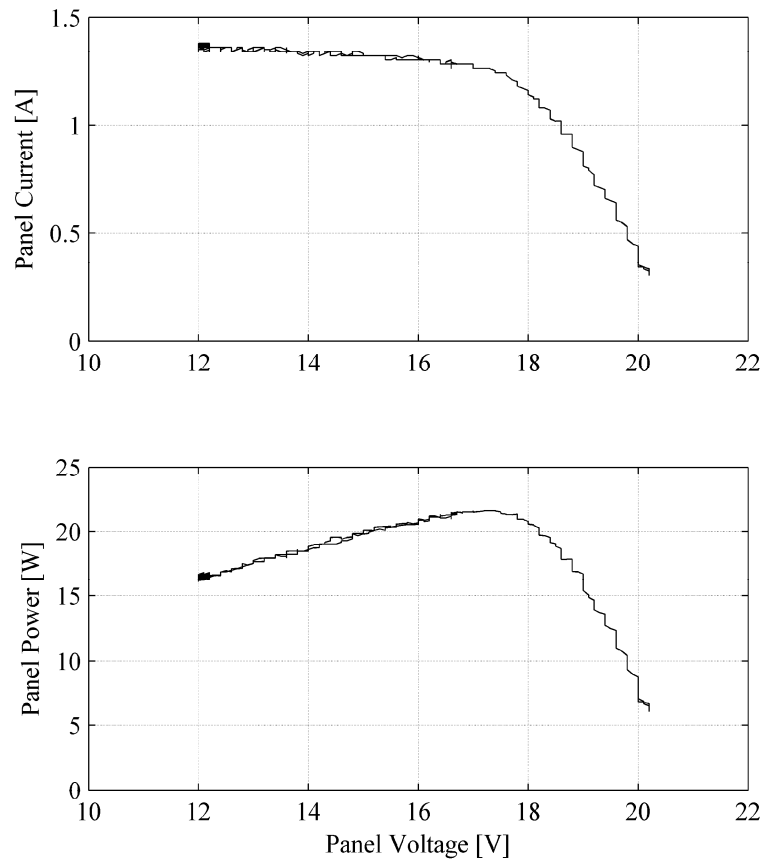


Fig. 5.3. Panel current and power as functions of voltage.

5.4.1. Energy storage effects

Since the cost function is a power quantity, stored energy can affect the performance of DRCC. A photovoltaic cell is an illuminated p-n junction, so it stores energy in the form of stored charge that varies with voltage. This can be modeled as a nonlinear junction capacitance. A typical MPPT uses a boost converter or other current-fed switching power converter. Panel current then has a primarily dc value with small triangular ac ripple at the switching frequency. The relationship between ripple current and changes in stored charge (capacitive voltage ripple) varies with the switching frequency. While the ripple current and voltage still contain information about the operating point, the capacitive phase shift complicates the process. No longer are voltage and current edges aligned as in Figs. 5.1 and 5.2. More realistic waveforms are shown in Fig. 5.4.

The edges of $\frac{di_{panel}}{dt}$ are exactly aligned with the switching function q , so

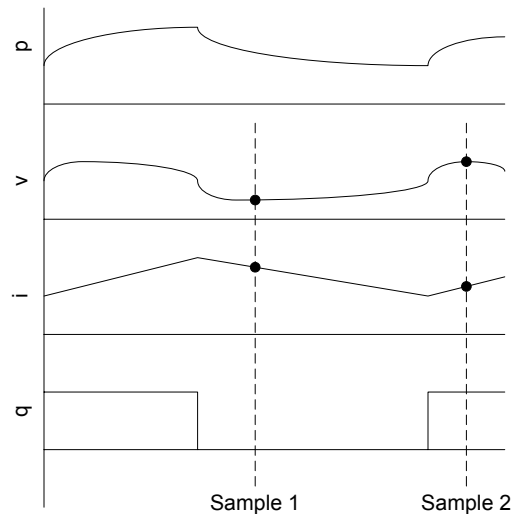


Fig. 5.4. Sample timing with panel capacitance effects. Waveforms shown are switching function q , panel voltage v , current i , and power p .

$$\text{sgn} \frac{di}{dt} = 2q - 1 \quad (5.27)$$

The microcontroller which generates the switching waveforms could easily generate sampling signals that are aligned with $\frac{di_{panel}}{dt}$. However, the control algorithm will continue to be effective at a much higher frequency if samples are aligned with edges of $\frac{dv_{panel}}{dt}$.

A study of the small-signal circuit shown in Fig. 5.5 reveals the relationship needed to generate sampling signals aligned with edges in $\frac{dv_{panel}}{dt}$. The resistance R in Fig. 5.5 represents the incremental resistance of the panel (the inverse of the slope of the I-V curve). Capacitance increases with voltage while resistance decreases [197]. Over a broad range near the maximum power point, the panel time constant RC is nearly constant. Multicrystalline silicon panels have been measured in various operating conditions to have a time constant of about 17 μs .

The applied current in Fig. 5.4 is triangular with a duty cycle governed by the switching waveform q . The appropriate sample time is when

$$\frac{dv_{panel}}{dt}(t_{sample}) = 0 \quad (5.28)$$

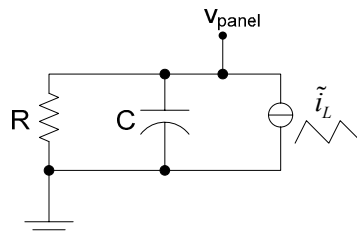


Fig. 5.5. Small-signal equivalent circuit of solar panel connected to a boost converter.

A solution of the differential equation that governs the circuit of Fig. 5.4 gives a sample time of

$$t_{sample} = DT + RC \ln \left(\frac{1 - \exp\left(\frac{(1-D)T}{RC}\right)}{(1-D)\left(1 - \exp\left(\frac{T}{RC}\right)\right)} \right) \quad (5.29)$$

That is, if time is reset to zero at the rising edge of q , the next sample should occur not at DT (the falling edge of q) but rather at t_{sample} . Similarly, if time is reset at the falling edge of q , replace D with $(1-D)$ everywhere in (5.29) to find the sample time that occurs after the next rising edge of q . Since the circuit is small-signal and linear, one equation determines the appropriate delay so that all samples align with the edges of (dv/dt) .

Equation (5.29) is too complicated for real-time calculation in an inexpensive 8-bit or 16-bit microcontroller. Math operations include exponentials, a division, and a

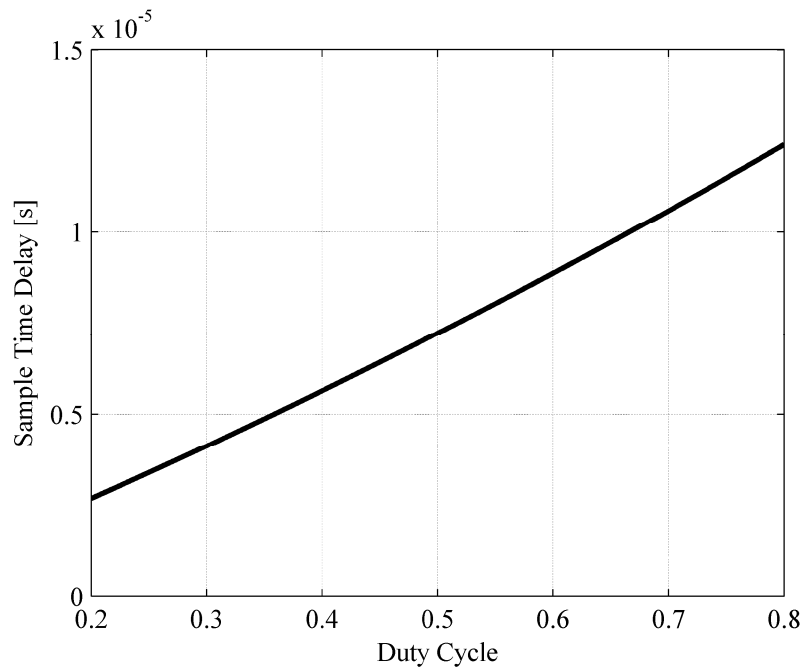


Fig. 5.6. Sample time delay as a function of duty cycle.

natural logarithm. Fortunately, a linear fit is adequate. Figure 5.6 shows a plot of (5.29) for $RC = 17 \mu\text{s}$ and $T = 40 \mu\text{s}$. For the experimental system, a piecewise linear fit was used. Maximum error was less than 2%.

5.4.2. Implementation and experimental results

An experimental MPPT was built to demonstrate the effectiveness of DRCC. The MPPT was a boost converter with a 3.4-mH inductor, an IRF3710 MOSFET, and a MBR1545CT Schottky diode. The solar panel was a Solec S-5136, with terminal characteristics shown in Fig. 5.3. The switching frequency was set to 25 kHz, a compromise between component sizes and detectable ripple. At lower frequencies, inductor size would be excessive, while at higher frequencies, panel capacitance would excessively attenuate and phase-shift voltage ripple measurements. A full schematic is shown in Appendix A.

The algorithm was implemented on an MSP430F148. The MSP430 family from Texas Instruments has a 16-bit fixed-point core and a variety of peripherals. The primary advantage of this family is low power consumption, which enables an effective MPPT for a relatively small panel. The MSP430F148 has a hardware 8-bit-by-8-bit (8x8) multiplier, a 12-bit analog-to-digital converter (ADC), and several timer channels that can implement PWM. Typical power consumption, including peripherals, is 1.2 mA at 3 V, or 3.6 mW. The full code listing is shown in Appendix F.

Voltage and current ripple are only a few percent of the total voltage and current. To achieve high signal integrity and sufficient ADC resolution, each signal was split into a dc component and an ac component. The gains on the ac components of voltage and current were 3.33 times greater and 32 times greater, respectively, than the gains on the

dc components. Sampling was performed with 74HC4066 switches. Current was sensed with a LEM LA55-P closed-loop Hall effect sensor with five primary turns, though a commercial implementation would likely use a current shunt instead. With this gain and filter configuration, an additional 10 dB of SNR was achieved for voltage and an extra 30 dB of SNR was achieved for current.

A mode-switching algorithm was implemented to improve robustness and overall performance. Many of the DRCC assumptions are easily enforced locally but break down at extreme operating points. Monotonicity of $\phi(u)$ is broken near short-circuit of the solar panel, and multiple maxima of J can occur near open-circuit when several cells are connected in series (as is common). Mode switching uses different control algorithms in different operating regimes to achieve global stability at the desired operating point.

Fractional open-circuit voltage (fractional V_{oc}), also referred to as constant voltage fraction (CVF), is a simple MPPT technique [198] that can be used to augment DRCC. Over a broad range of operating conditions, the maximum power point occurs where the panel voltage is some fraction k_{CVF} of the open-circuit voltage V_{oc} . More recent work [199] has shown that a variable fraction achieves higher accuracy. Another option would be to use a fraction of short-circuit current I_{SC} , which was also shown to be more accurate in [200]. However, the main reason to augment DRCC with another MPPT technique is to initialize DRCC within the basin of attraction of the true maximum power point, so the simplest CVF technique is adequate. Use of a sampled V_{oc} , rather than a fixed voltage, compensates for temperature variation and panel aging.

The complete algorithm has three modes:

1. The converter is turned off for a predetermined time that is sufficient for the panel to reach V_{oc} . At the end of this time, V_{oc} is sampled.
2. The CVF algorithm is enabled. The panel voltage converges to $k_{CVF}V_{oc}$.
3. The DRCC algorithm is enabled. Since the initial conditions are near the maximum power point, convergence is quick.

This sequence repeats after a predetermined time. In the experimental system, the open-circuit time is 10 ms, the CVF time is 230 ms, and the DRCC time is about 3 s.

Figure 5.7 shows panel current, voltage, and power with the mode-switching algorithm active. At $t = 0$, the system is in mode 1, open-circuit. For mode 2, k_{CVF} was set to 0.625 to demonstrate the large basin of attraction for DRCC. A more appropriate setting for a commercial version would be about 0.8. The trace in Fig. 5.7(c) shows that the panel sweeps through the maximum power point (21.6 W). While the CVF algorithm is in use, the microcontroller does not sample current, so there is no stored knowledge of the maximum power point. After 230 ms, the DRCC algorithm is enabled. The final operating point, where $v_{panel} = 0.824 \times V_{oc}$, is consistent with manufacturer's data for the maximum power point. The steady-state power, 21.4 W, is 99.1% of the true maximum.

A separate work [197] studied an interesting method to achieve good ripple over a wide range of currents. The magnitude of the current ripple depends on the switching frequency and the inductor value. Large ripple on a solar panel results in greatly reduced output power, since the panel is far away from the maximum power point for a significant portion of the switching period. If the inductor is chosen for appropriate ripple at low light levels and used across a wide range of light levels, its physical size would be large. The method in [197] uses a reconfigurable inductor to minimize both size and ripple

current over a wide operating range. This approach should be considered in future DRCC systems.

5.5. Summary

In this chapter, DRCC, a new discrete-time online optimization method, was derived and explored. DRCC has the same theoretical basis as the existing RCC algorithm. Knowledge of converter dynamics allows a simplification when the continuous-time law is converted to discrete-time. The new law was proven to be stable.

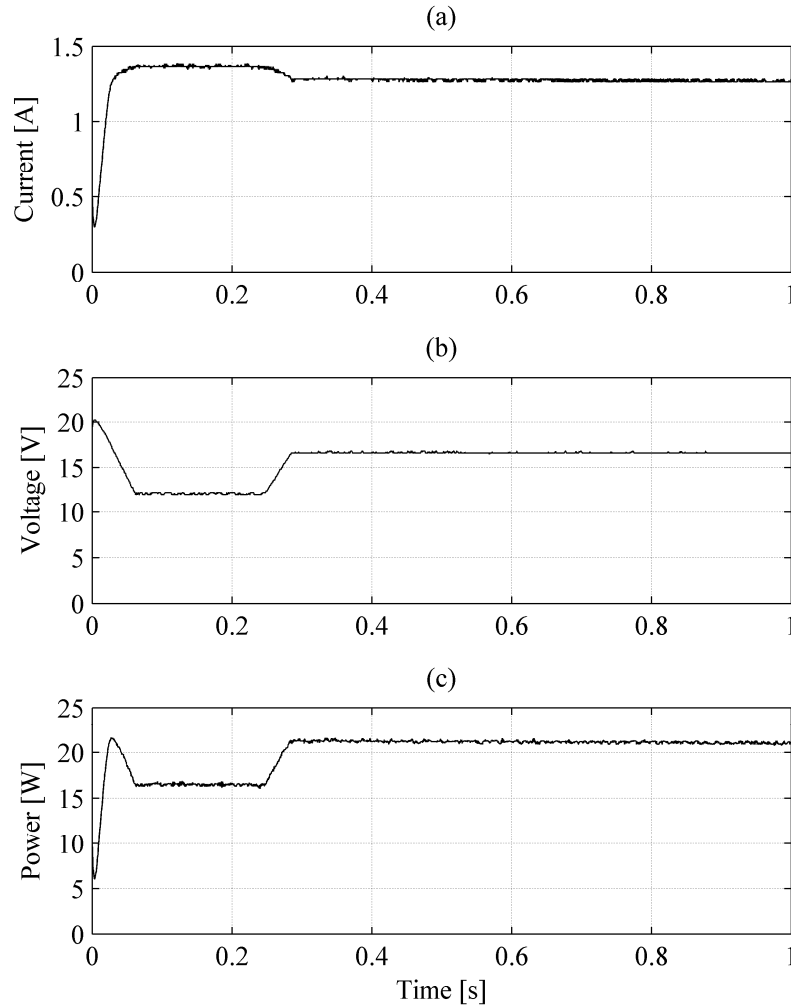


Fig. 5.7. Mode-switching algorithm with DRCC, experimental results: panel current (a), panel voltage (b), and panel power (c).

In equilibrium, the optimum operating point is enclosed by the ripple band.

DRCC was demonstrated in an MPPT for photovoltaic panels. Tracking accuracy exceeded 99%. A mode-switching algorithm that used the fractional V_{oc} method for periodic reinitialization improved robustness and ensured that the MPPT would converge to the true maximum power point.

DRCC is a general-purpose technique. Future work would apply this method to other applications. For example, DRCC can also be used for motor efficiency maximization. A motor running below rated load has excessive losses if operated with nominal flux. RCC has been previously explored for motor power minimization. DRCC has similar advantages for the motor application as for the PV application, if suitable observers can be constructed.

Another topic for future research is parameter estimation to better mitigate energy storage effects. The method presented used offline knowledge of the panel time constant to precalculate sample timing. Another approach is to continually monitor waveforms and adjust to actual system parameters. The Kalman filter techniques presented in Chapter 4 apply, if a computationally efficient model of the panel voltage waveform can be constructed. Ultimately, the goal is to determine the sample times, not the panel parameters, so a simplistic model can likely be effective.

CHAPTER 6

SUMMARY AND CONCLUSIONS

The objective of this dissertation is to provide a set of tools for future digital control applications. To achieve all of the benefits of digital hardware, Generation 4 approaches are needed. These require new modeling frameworks and new perspectives on power electronics. Three new methods are shown.

Although previous researchers have assumed that inductor current and capacitor voltage time scales are separate, a singular perturbation analysis enabled a formal separation between fast and slow time scales in a switching power converter. A rigorous analysis gave several criteria for time-scale separation in boost, buck, buck-boost, and flyback converters. The analysis was performed in the continuous-time and discrete-time domains and was applied to both constant-resistance and constant-power loads. The tool relates primarily to component selection and secondarily to sample rate selection. Designers can use this tool as a check before designing separate control loops, as a basis to choose the inductor and capacitor, or as a requirement for the sampling rate of a digital controller. Two further techniques were developed that use information from the fast time scale in system control.

Kalman filters were used in place of traditional observers to design a PFC controller without current sensors. While a traditional power converter control problem might use inductor current or capacitor voltage as states, the Kalman filter-based system used two or three waveform parameters as states: magnitude and phase of ac voltage, plus a dc voltage. The complete system had five states, divided into two Kalman filters with two and three states, respectively. A phasor-based controller using the Kalman filter

states was shown experimentally. This tool relates directly to control of power converters, particularly systems with reduced sensor count or sample rate.

A discrete-time online optimization technique, DRCC, was derived from RCC, a well-established continuous-time technique. DRCC was created with knowledge of plant dynamics and precisely-timed samples that extract information about the system operating point. Two samples of a cost function aligned with the extremes of switching ripple in a state variable were used to determine which direction to change the input. A generic stability proof was given. The new technique was applied to a photovoltaic MPPT, where the ripple variable was the panel voltage and the cost function was the panel power. This MPPT showed all of the salient features of DRCC: reduced sample rate (two samples per switching cycle), mitigation of energy storage effects, and multimode operation. Tracking effectiveness of 99% was demonstrated. DRCC can be applied to many of the same optimization problems as RCC, and potentially others that are inconvenient to implement in continuous-time. This tool relates primarily to optimization and secondarily to control.

At a recent conference (IEEE Power Electronics Specialists Conference 2007), there was a rap session that discussed the future of digital control. There is no longer any question of whether digital elements will be used in power converters—they are already widespread, particularly Generation 1 devices (digital power management). The larger question is what form future digital approaches will take. As long as designers think in terms of Generation 1 or 2 devices, the advantages are modest. If instead designers consider Generation 3 approaches, as are used in the motor drive world, or Generation 4 approaches, as discussed in the present work, digital controllers have huge advantages for

many applications. Digital controllers can improve performance, robustness, and efficiency, and can mitigate noise and other unwanted disturbances easily.

6.1. Future Work

Singular perturbation analysis can be extended from open-loop plant dynamics to closed-loop control problems in power electronics. A typical power converter controller has one or more states in addition to the states of the plant. The singular perturbation analysis can be applied to voltage mode, current mode, and sensorless current mode analog controllers, as well as to simple digital methods, such as predictive current control.

Kalman filters can be used to extract useful information from any noisy system. Future work could explore application to active filters, dc-dc converters with high switching frequencies, and large systems of interconnected power converters. Also, Kalman filters could be used for system identification—a supervisory role outside the main control loop. For example, a Kalman filter might be used for load estimation or solar panel time constant estimation.

The next step in DRCC development would be to apply it to systems with multiple goals. For example, an ASD must control an induction motor to deliver the commanded torque or speed at the maximum efficiency. Previous research has shown that the control problem can be partitioned so that RCC can be used to maximize efficiency. Implementation could be simplified with the use of DRCC instead. The motor control problem requires more research to formulate an appropriate observer. Just as panel capacitance affects an MPPT, motor inductance affects an efficiency maximizer. System identification or other supervisory methods could address the energy storage problem.

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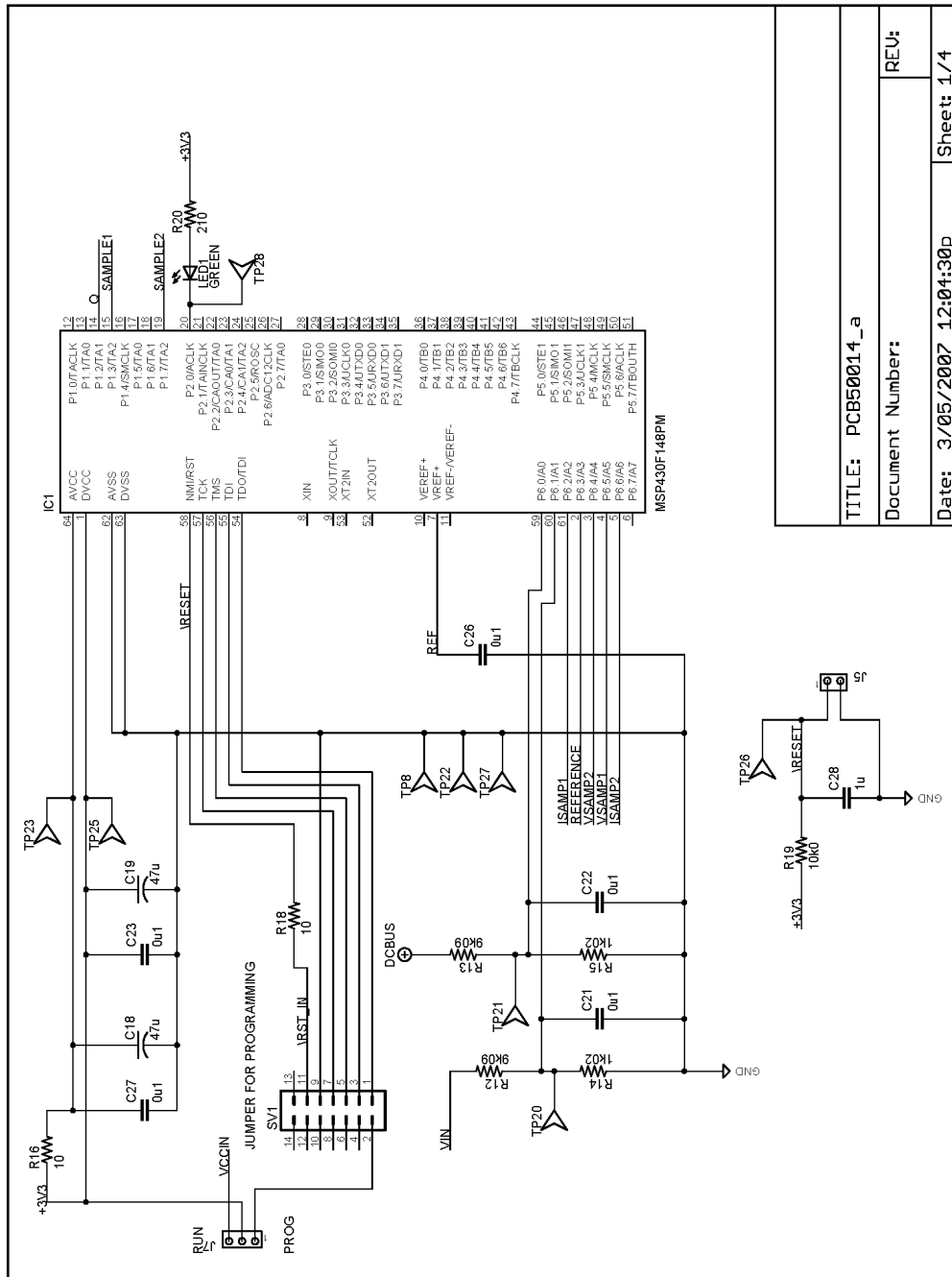
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APPENDIX A

SCHEMATIC (PCB50014 REV A) FOR DRCC EXPERIMENTS

This schematic was used for the experiments summarized in Section 5.4.2.



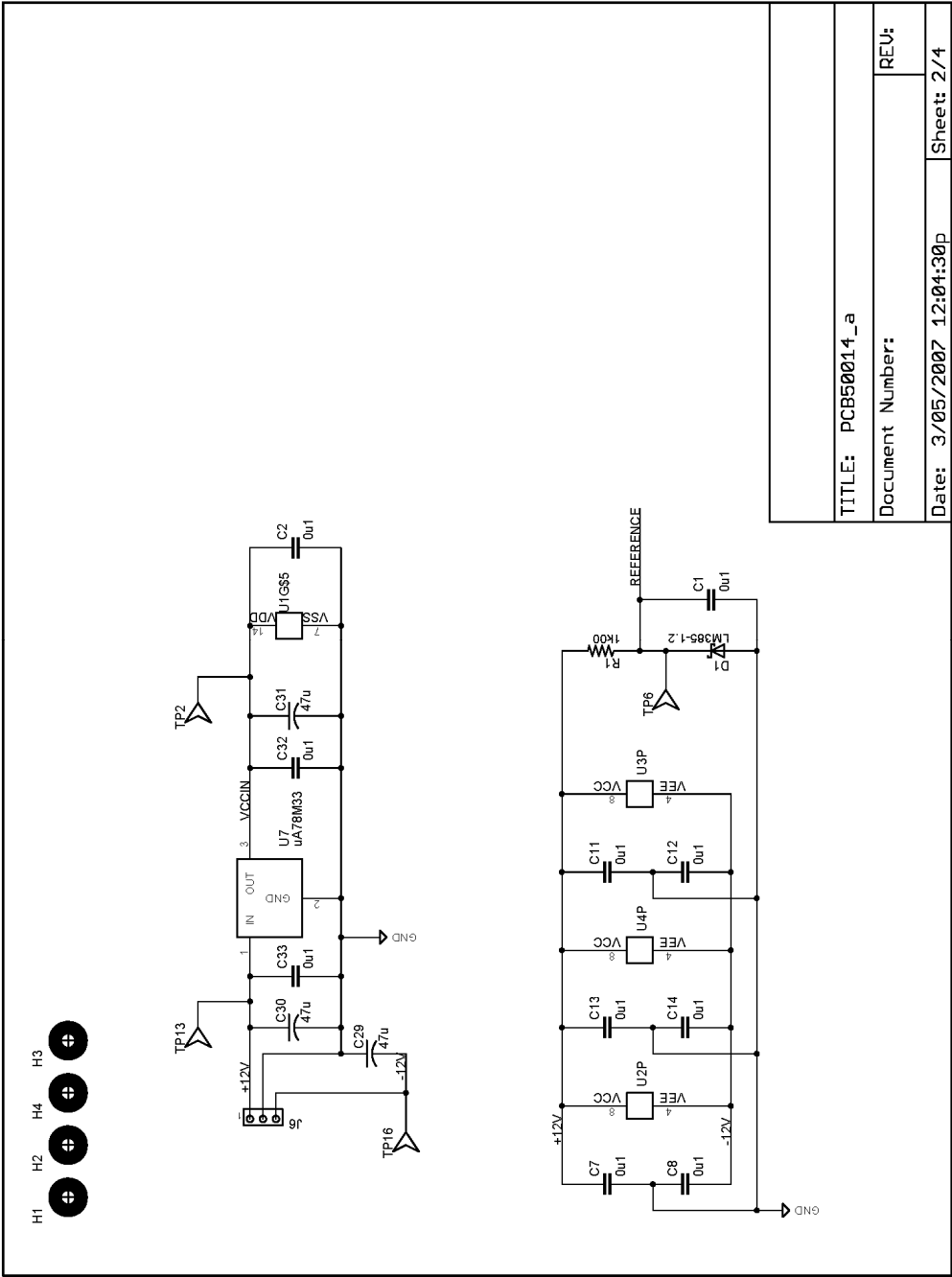
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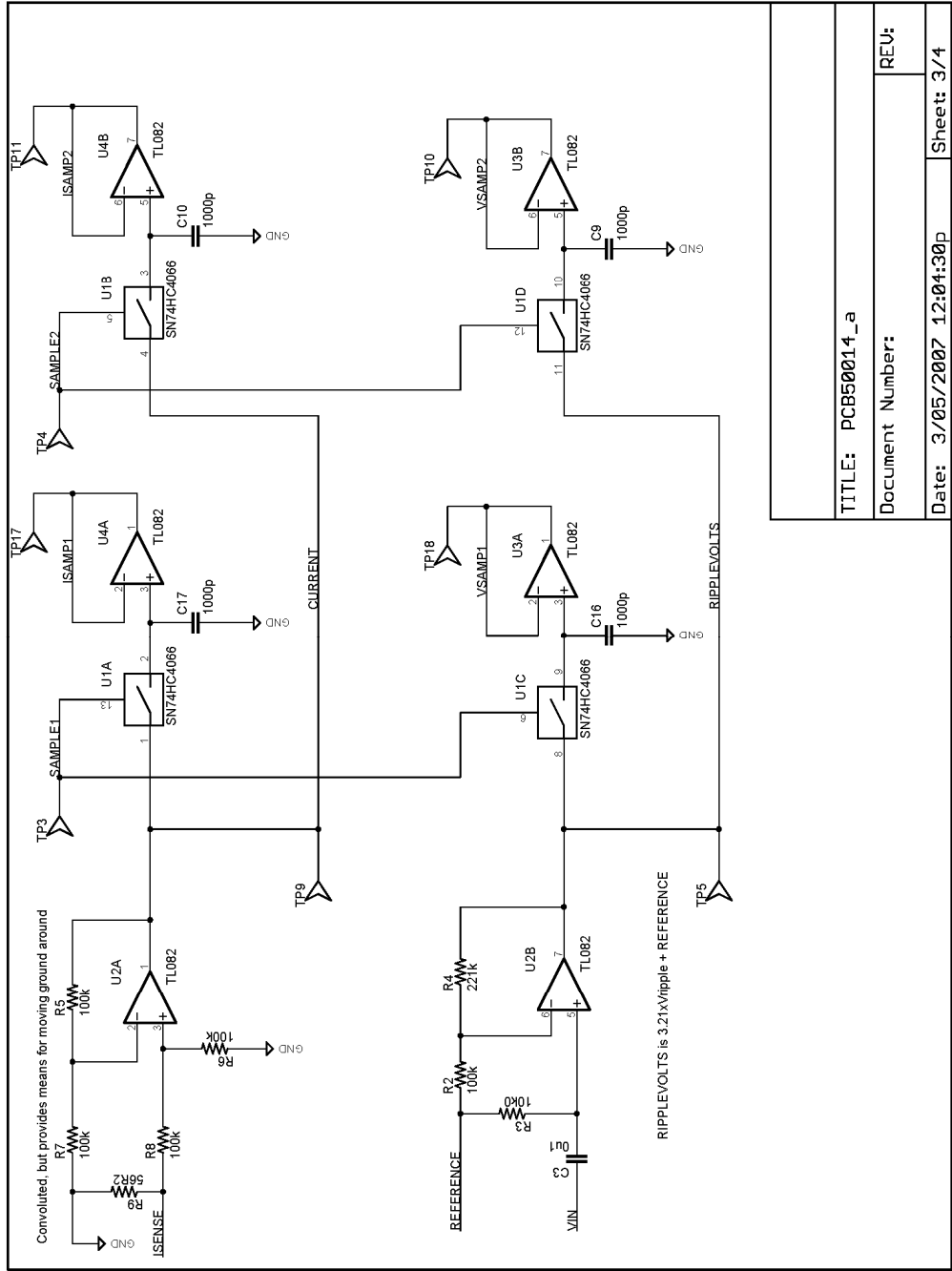
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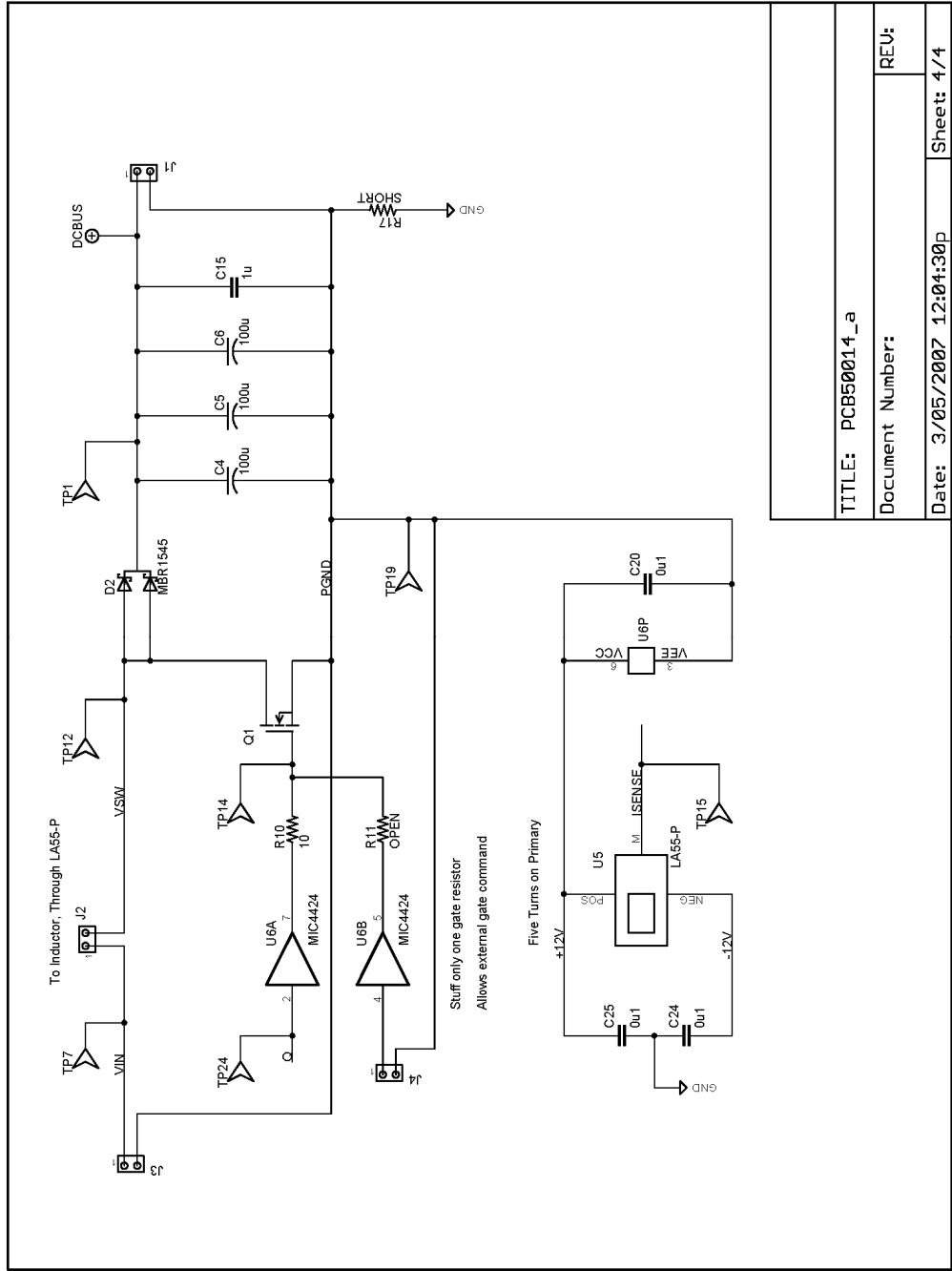
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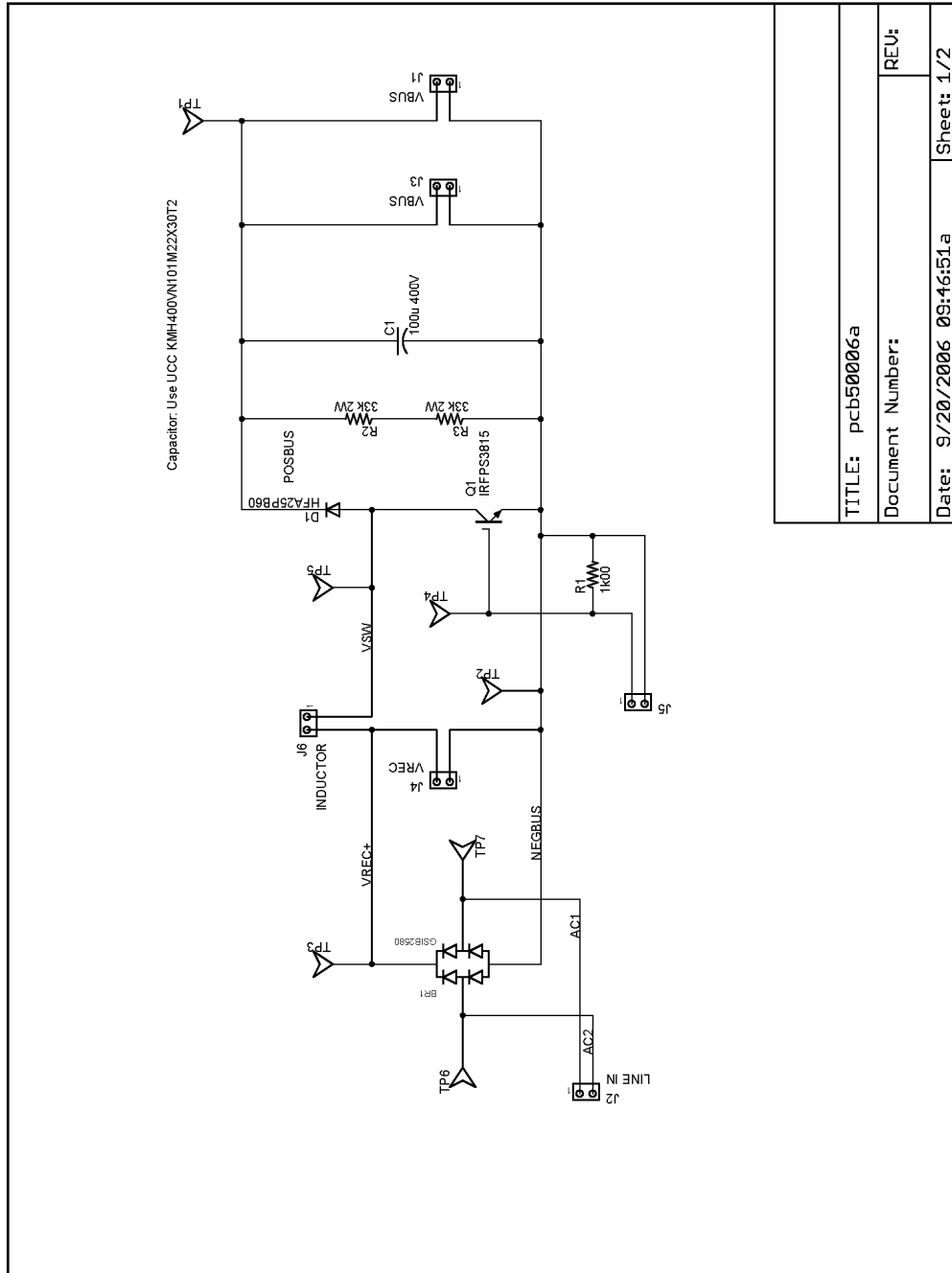


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APPENDIX B

SCHEMATIC (PCB50006 REV A) FOR PFC EXPERIMENTS

This schematic was used for the experimental results shown in Section 4.3.



TITLE: pcb50006a

Document Number:

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APPENDIX C

MATHEMATICA CODE FOR KBM AND SINGULAR PERTURBATION ANALYSIS

The first part of this code, which performs a KBM average, is taken from [11].

```

x={vCnorm,iLnorm};
T={0,duty*p,p};
nconfig=2;
amat={{1,h2},{-h2/ε,(δ0+h2*Rc/R)/ε}};
bmat={{-w2,(Rc+R)*w1/(ε*R)-h2*w2*Rc/(ε*R)}};

n=Length[x];
a={(amat/.{h1→1,h2→0}),(amat/.{h1→0,h2→1})};
b={(bmat/.{h1→1,h2→0}),(bmat/.{h1→0,h2→1})};

rhs=Table[a[[i]].x+b[[i]],{i,nconfig}];

AVERAGE[f_]:=Cancel[(1/p)
Sum[Integrate[f[[id0]],{t,T[[id0]],T[[id0+1]]}],{id0,nconfig}]];

PDER[fv_,v_]:=Table[D[fv[[id1]],v[[jd1]]],{id1,n},{jd1,n}];

KBMalgorithm[rhspsi_,Gold_,psiold_,Golder_,psiolder_]:=Block[{i},
  G=AVERAGE[rhspsi];
  psidi=Simplify[Table[Integrate[rhspsi[[i]]-G-
PDER[psiolder[[i]],x].Gold-
PDER[psiold[[i]],x].Golder,t],{i,nconfig}]];
  psibc={psidi[[1]]};
  Do[AppendTo[psibc,Cancel[psidi[[i]]+(psibc[[i-1]]/.t→T[[i]])-
(psidi[[i]]/.t→T[[i]])]],{i,2,nconfig}];
  psiavg=AVERAGE[psibc];
  psi=Table[psibc[[i]]-psiavg,{i,nconfig}];];

zerovec=Table[0,{i,n}];
zeromat=Table[zerovec,{i,nconfig}];

KBMalgorithm[rhs,zerovec,zeromat,zerovec,zeromat]
G1=Simplify[G]
Ψ1=Simplify[psi];
Ψavg1 = Simplify[psiavg];
Ψd1l = Simplify[psidi];

apsi=Table[a[[j]].Ψ1[[j]],{j,nconfig}];
KBMalgorithm[apsi,G1,zeromat,zerovec,Ψ1]
G2=Simplify[G]
Ψ2=Simplify[psi];

apsi=Table[a[[j]].Ψ2[[j]],{j,nconfig}];
KBMalgorithm[apsi,g2,Ψ2,g1,Ψ1]
G3=Simplify[G]
f = G1[[1]]+G3[[1]]
g = ε*(G1[[2]]+G3[[2]])

```

```

intermediate = Solve[g==0,iLnorm]
φ0 = (iLnorm /. intermediate)[[1]]
φ1 = (1/D[g,iLnorm])*(D[φ0,vCnorm])*(f /. iLnorm → φ0)
ηrhs = (g /. iLnorm → (φ0 + ε*φ1 + η)) - ε*(D[φ0,vCnorm])*(f /.
iLnorm → (φ0+η));
simpleηrhs = Simplify[ηrhs]
ηcoeff = D[simpleηrhs,η]
infinitef = Simplify[simpleηrhs /. p → 0]
Solve[D[infinitef,η]==0, ε]
infinitefφ0 = φ0 /. p → 0
infinitefφ1 = φ1 /. p → 0
Simplify[infinitefφ1]
infinitefηcoeff = ηcoeff /. p → 0
Simplify[infinitefηcoeff]

```

APPENDIX D

SETUP CODE FOR SENSORLESS PFC

Execute this code in MATLAB prior to running the Simulink block diagram

shown in Appendix E, in order to reproduce the results of Section 4.3.

```
Tripple = 1/120;
Vpk = 140;
Vbus = 190;
Cbus = 0.0016;
Rc = .11;
Lin = .003;
RLact = 1.33;
RLest = RLact;
Tcycles = 1500;
T = 2*Tcycles/75e6;
fs = 1/T;
acq = 8192*2;
scale = 1/(6*acq);
Iout = 0.6;

% Gains; v7.0.4 does not accept fixed-point format
myinf = 500; % replaces inf in saturation
limits

Vturnon = 120; % bus voltage threshold to
enable PFC stage
Vturnoff = 90; % threshold to turn off
Overvoltage = 215; % overvoltage threshold
OVOK = 195; % recover from overvoltage
delay1 = 1; % delay from exceeding Vturnon
to precharge
delay2 = delay1+.1; % delay from exceeding Vturnon
to enable
Eref = 0.5*Cbus*Vbus^2; % reference bus capacitor
energy
Eon = 0.5*Cbus*Vturnon^2; % pre-loaded energy

ADCscale_Vbus = 3.3*3/(.013*2^12); % scales integer to
real Vbus
ADCscale_Vrec = 3.3*3/(.018*2^12); % scales integer to
real Vrec

variance = 9;
P0 = [variance 0.1 0.1 0.1];
```

```

R = variance;
H = [1 0];
P22 = (377*T)^2 / 12;
VinP0 = [variance 0 0 P22];
mybignum = 2^16;

% ADC vars
Gv = 0.01;
Vadc = 2.5;
nbits = 12;

MaxTime = 0.97*pi;
P0Vo = [variance 0 0 0 100*w*w*T*T 0 0 0 100];
Idc = 10;
phimax = 0.3;
QVo = zeros(9,1);
QVo(1) = (Idc*T/(6*pi*Cbus))^2;
QVo(5) = (phimax*T/(Tripple))^2;
QVo(9) = (Idc*T/(3*Cbus))^2;

QVo(2) = 0.1*sqrt(QVo(1)*QVo(5));
QVo(3) = 0.3*sqrt(QVo(1)*QVo(9));
QVo(4) = QVo(2);
QVo(6) = 0.1*sqrt(QVo(5)*QVo(9));
QVo(7) = QVo(3);
QVo(8) = QVo(6);

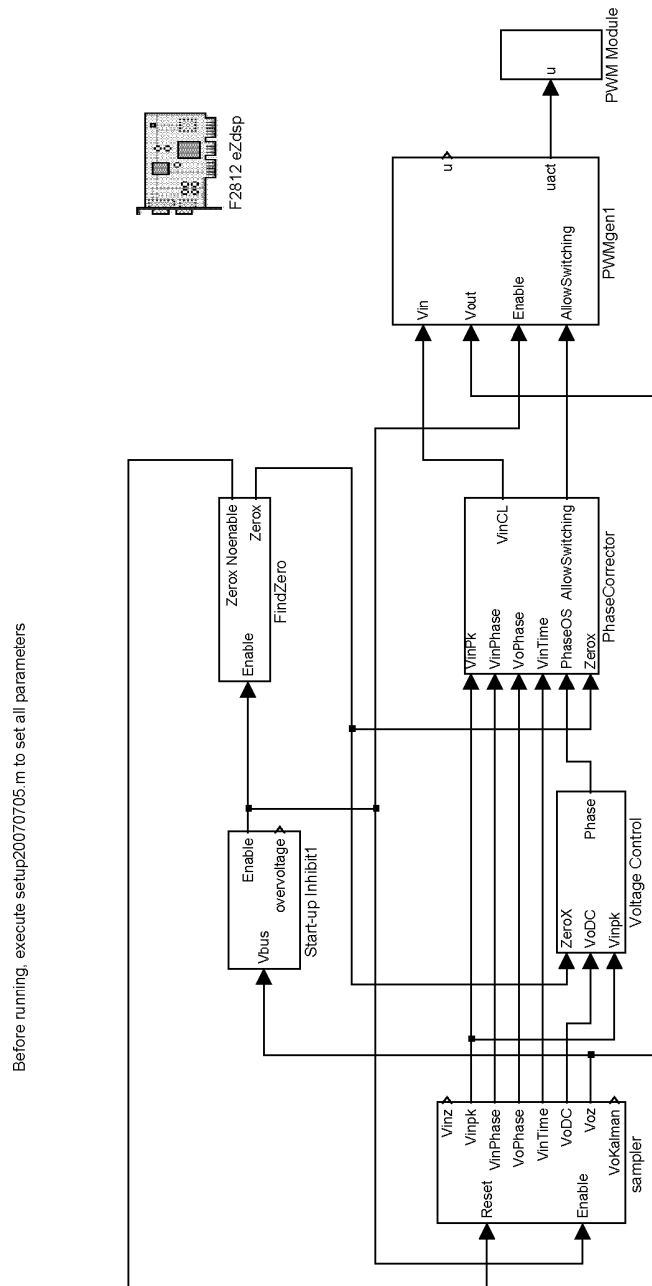
GVpk2 = -Tripple/(2*w*Lin);
GE = Cbus/2;
Gphase = 0.001;
GphaseI_zerox = Gphase * Tripple/T;
GphaseP = 10;
Ginv = 1/(GVpk2 * 170 * 170);

```

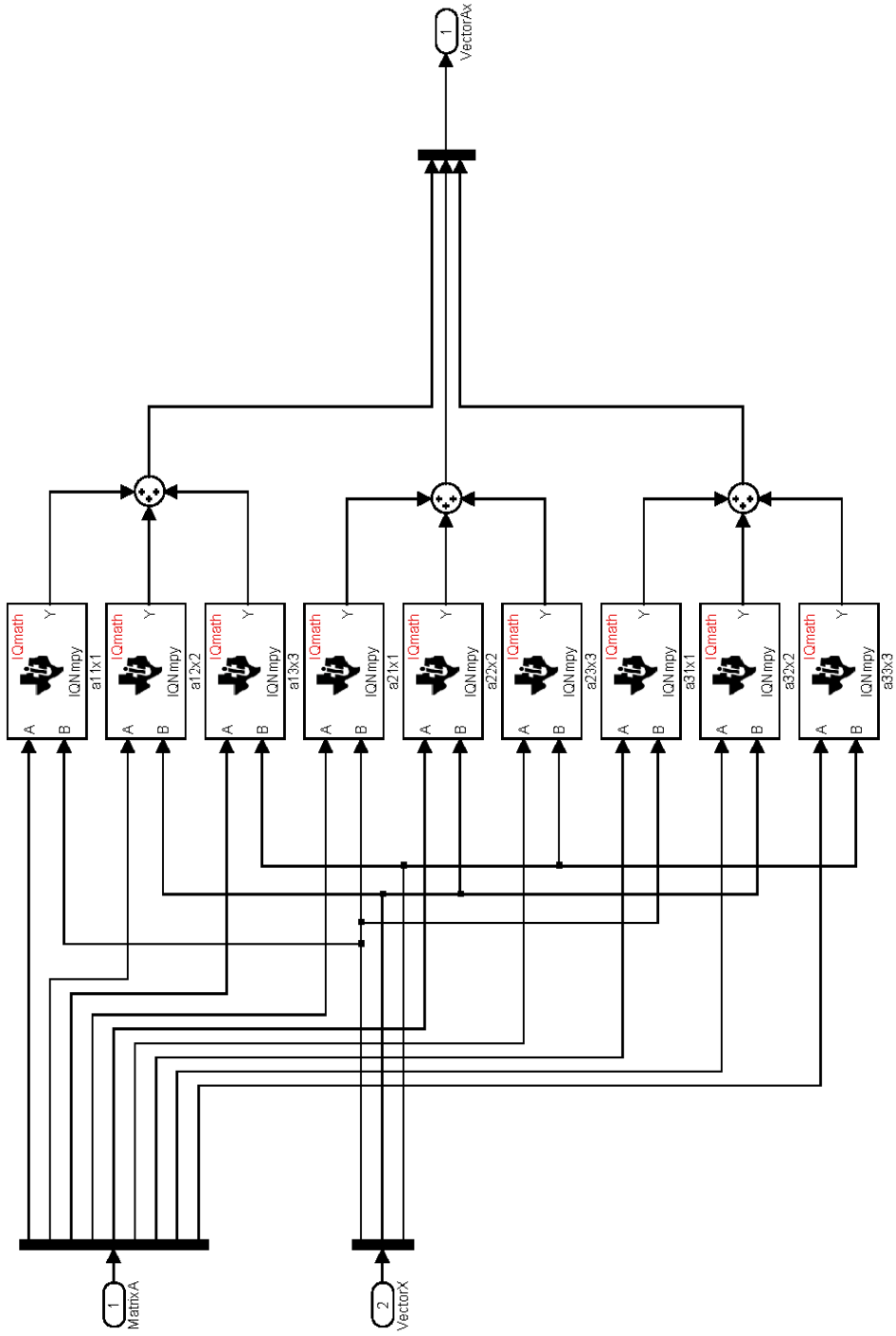
APPENDIX E

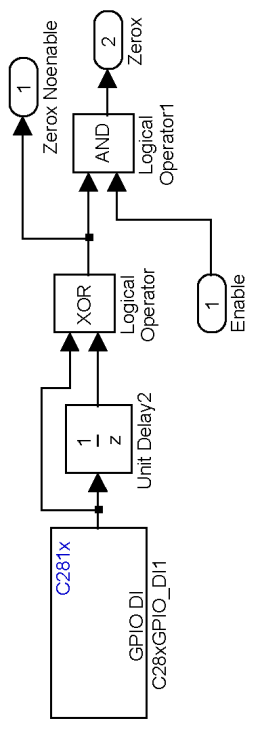
HIERARCHICAL SIMULINK BLOCK DIAGRAM FOR SENSORLESS PFC

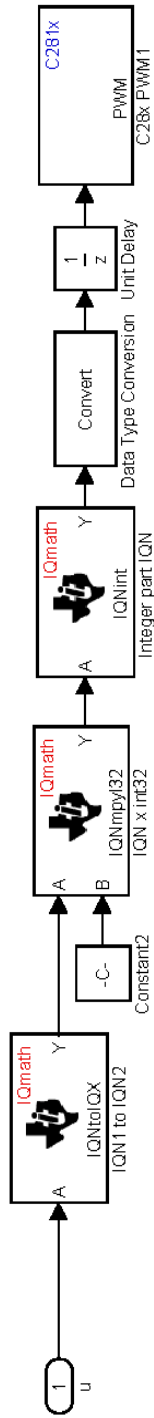
First, execute the setup code of Appendix D. Then this Simulink block diagram can be used to generate and compile C code for the results of Section 4.3.

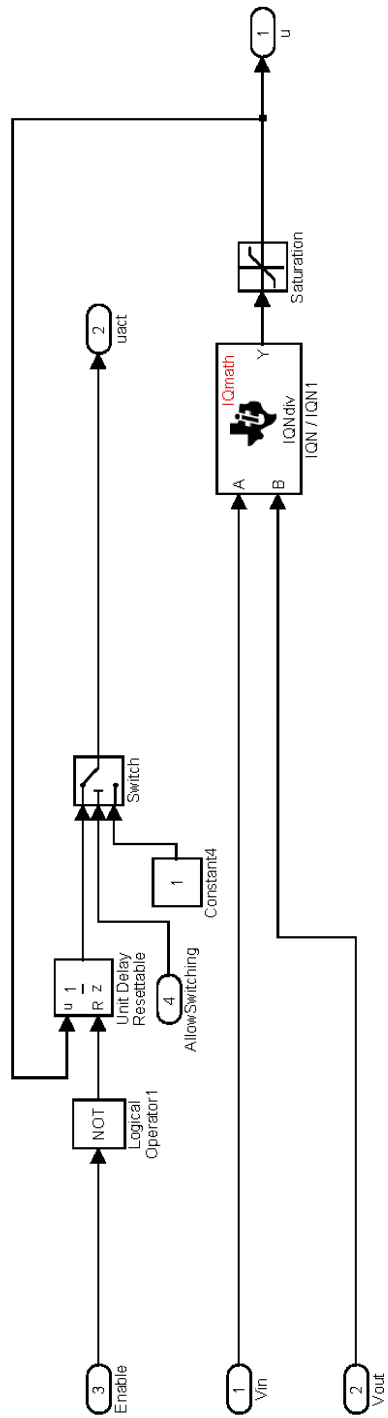


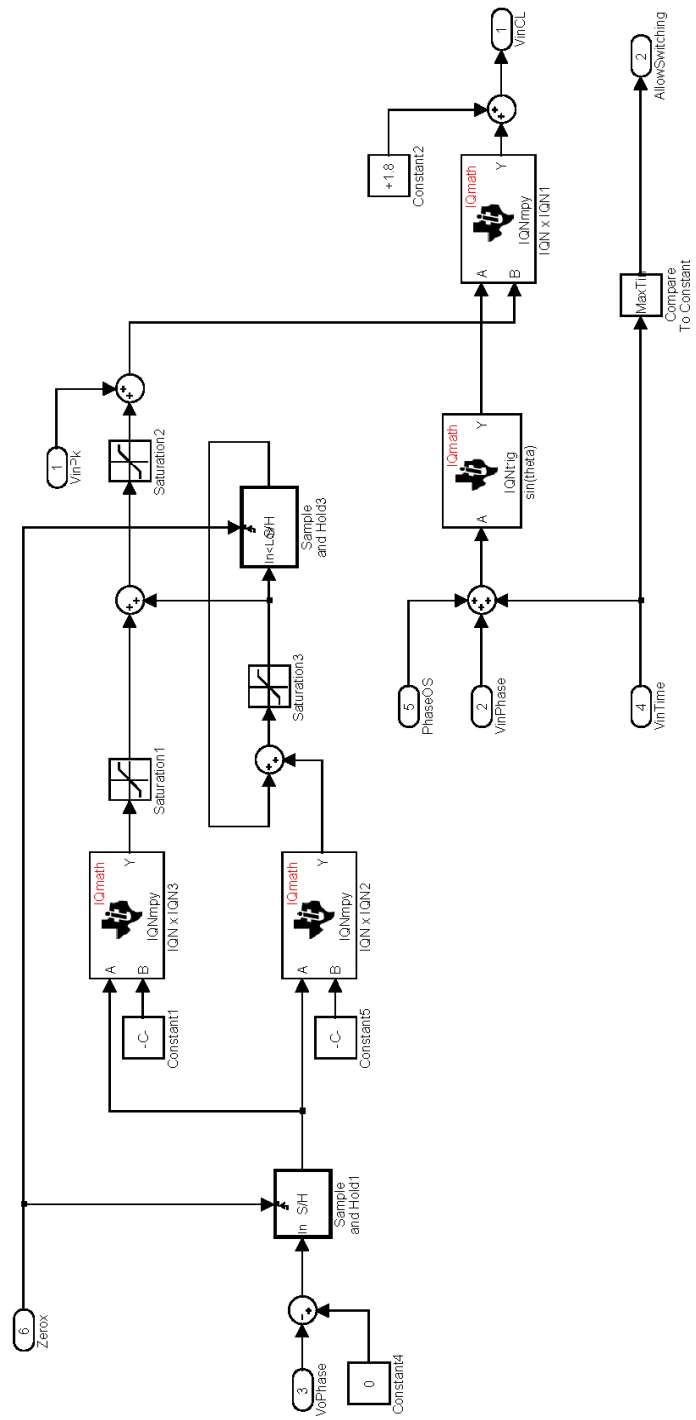
Matrices are stored as vectors, [a1_1,a12,a13,a21,a22,a23,a31,a32,a33]

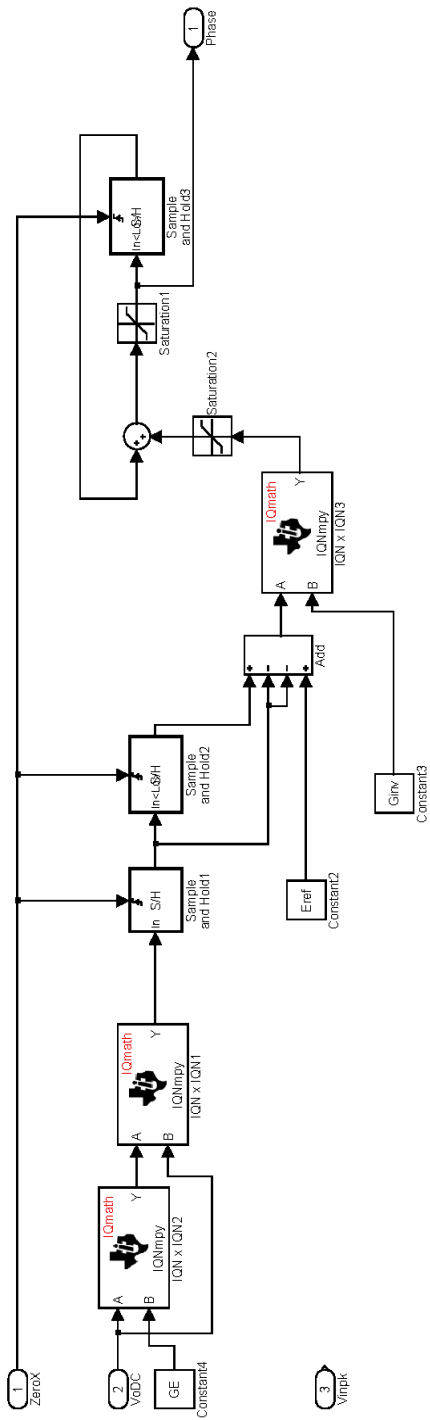


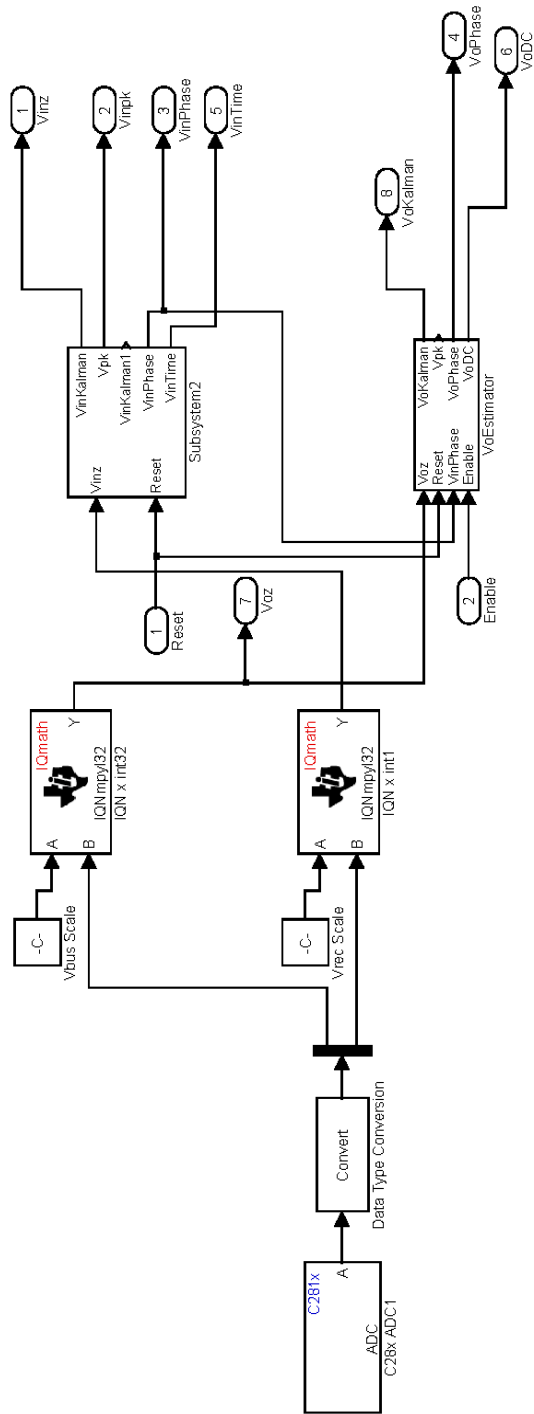




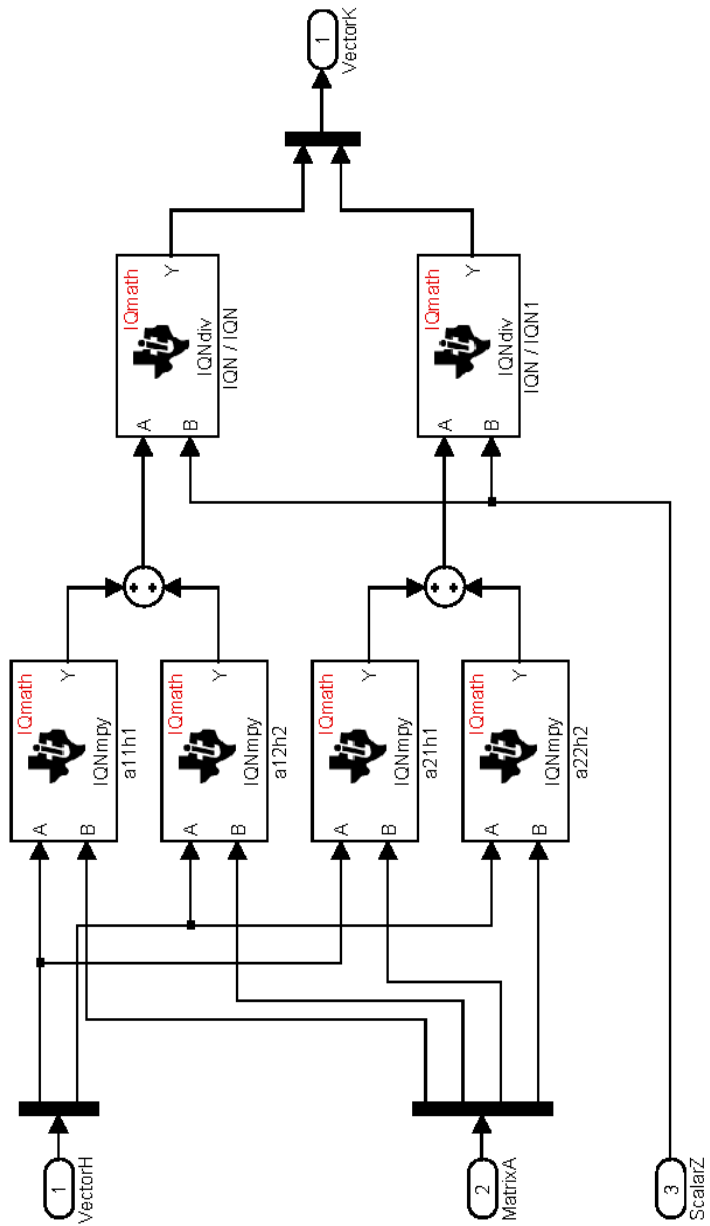




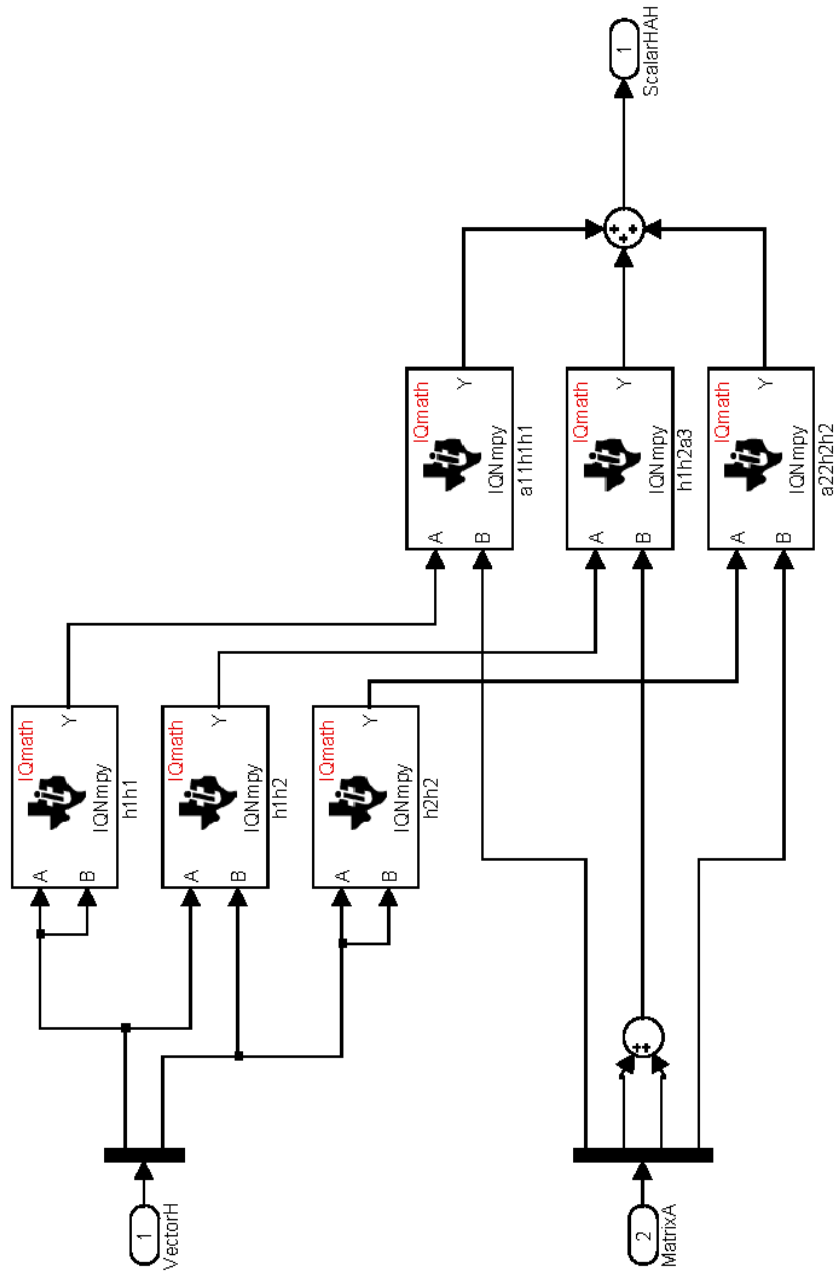




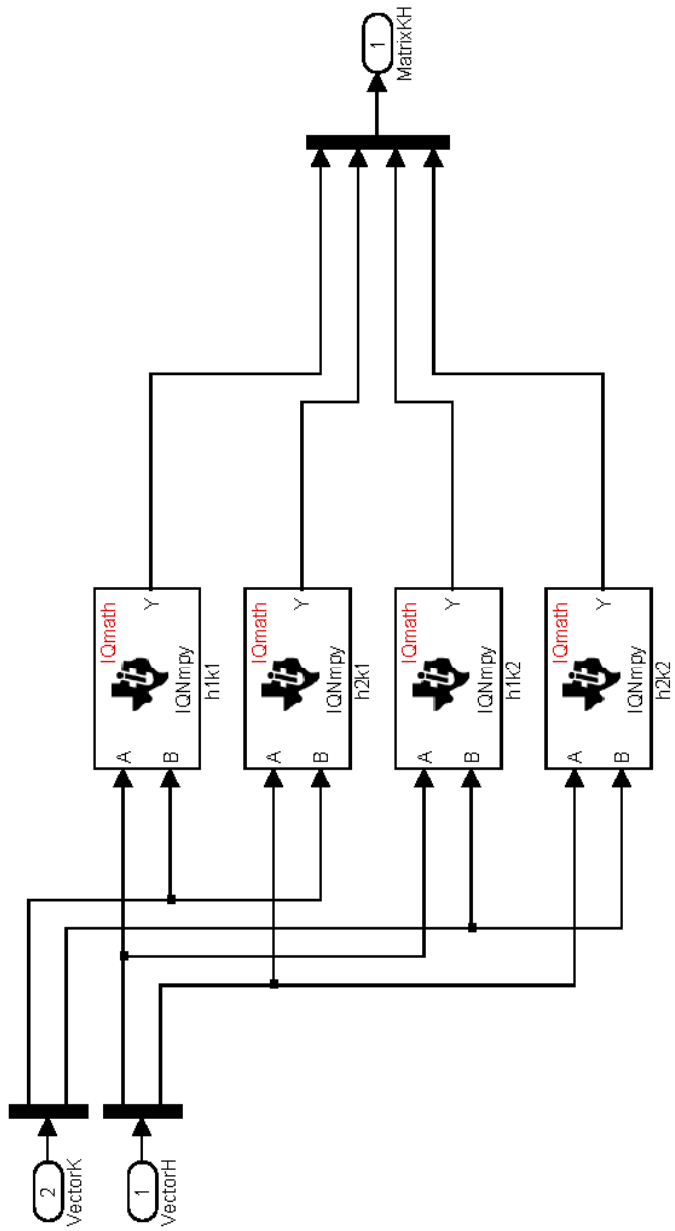
Matrix is stored as a vector, [a11, a12, a21, a22]
 Computes $K=AH^T Z$



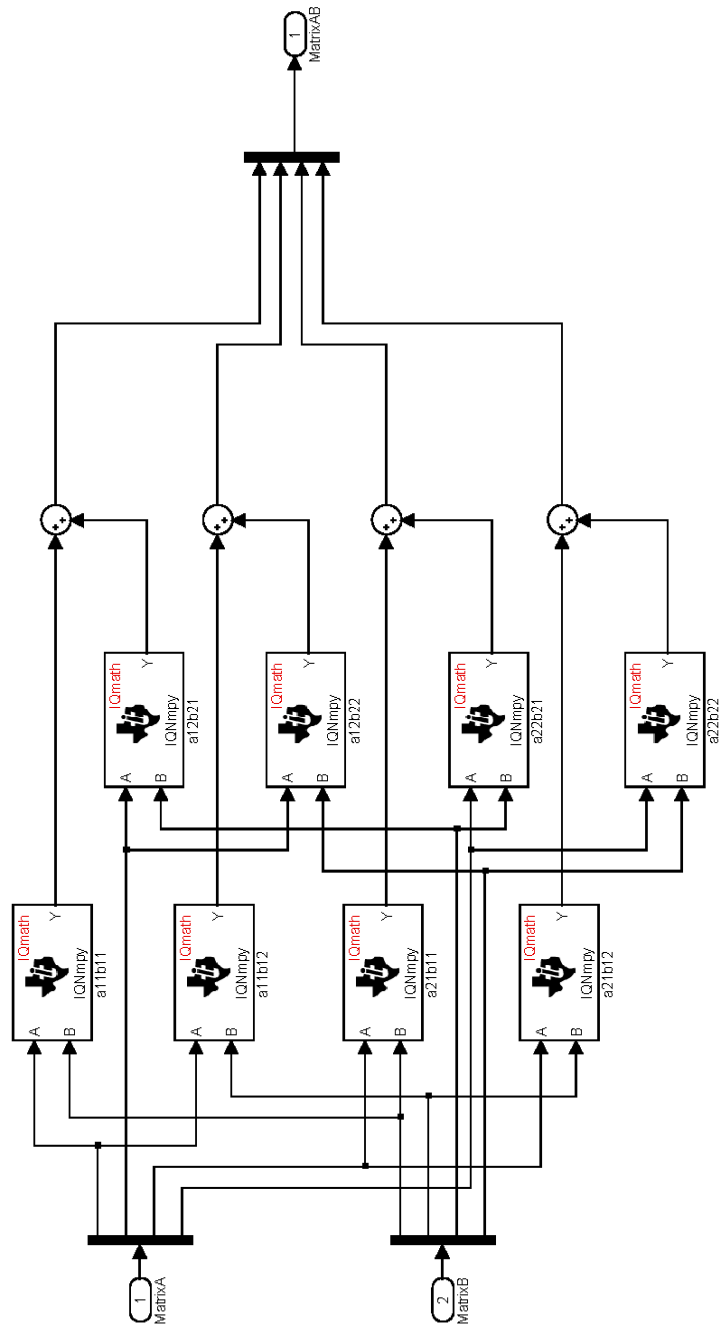
Matrix is stored as a vector, [a11,a12,a21,a22]
 Computes 'HAH'



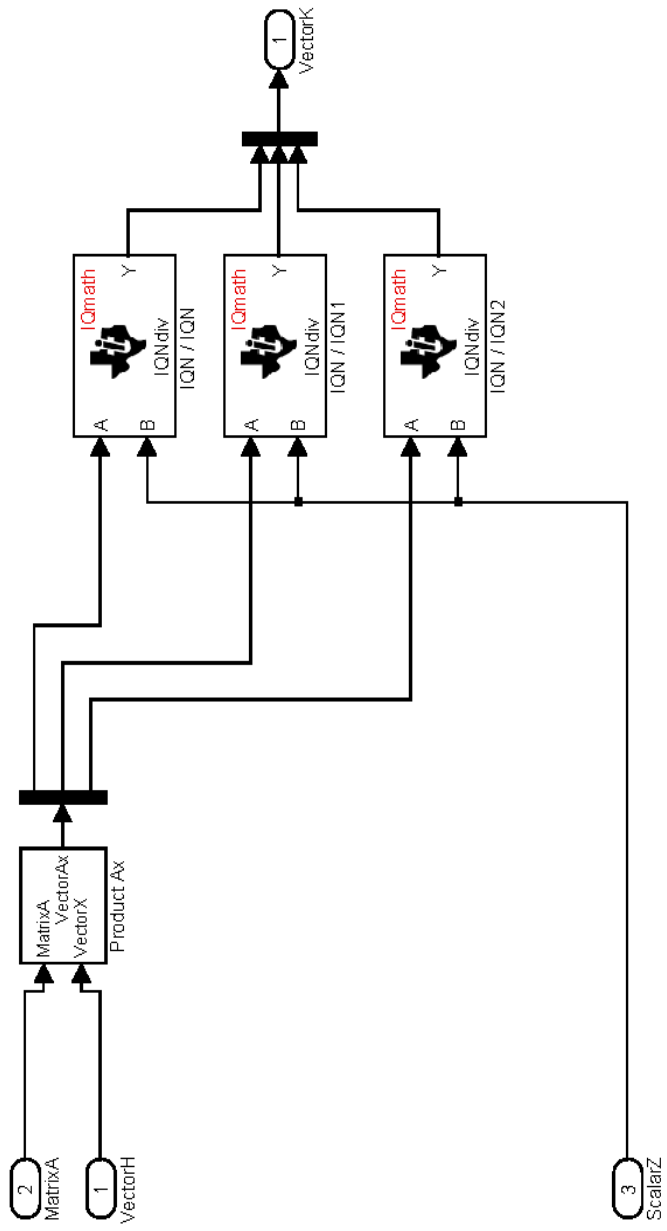
Matrix is stored as a vector, [a11,a12,a21,a22]
 Computes KH



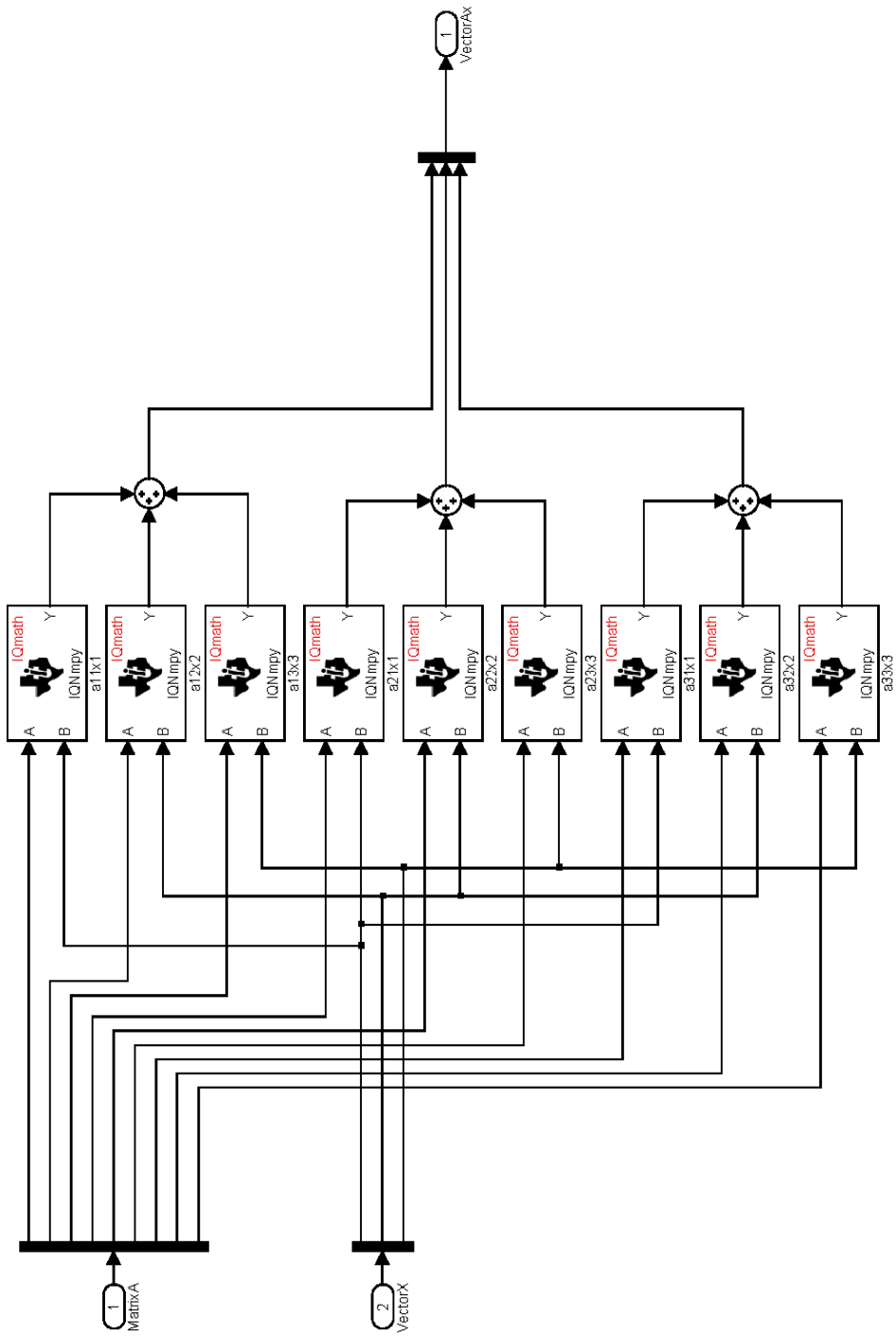
Matrices are stored as vectors, [a11, a12, a21, a22]



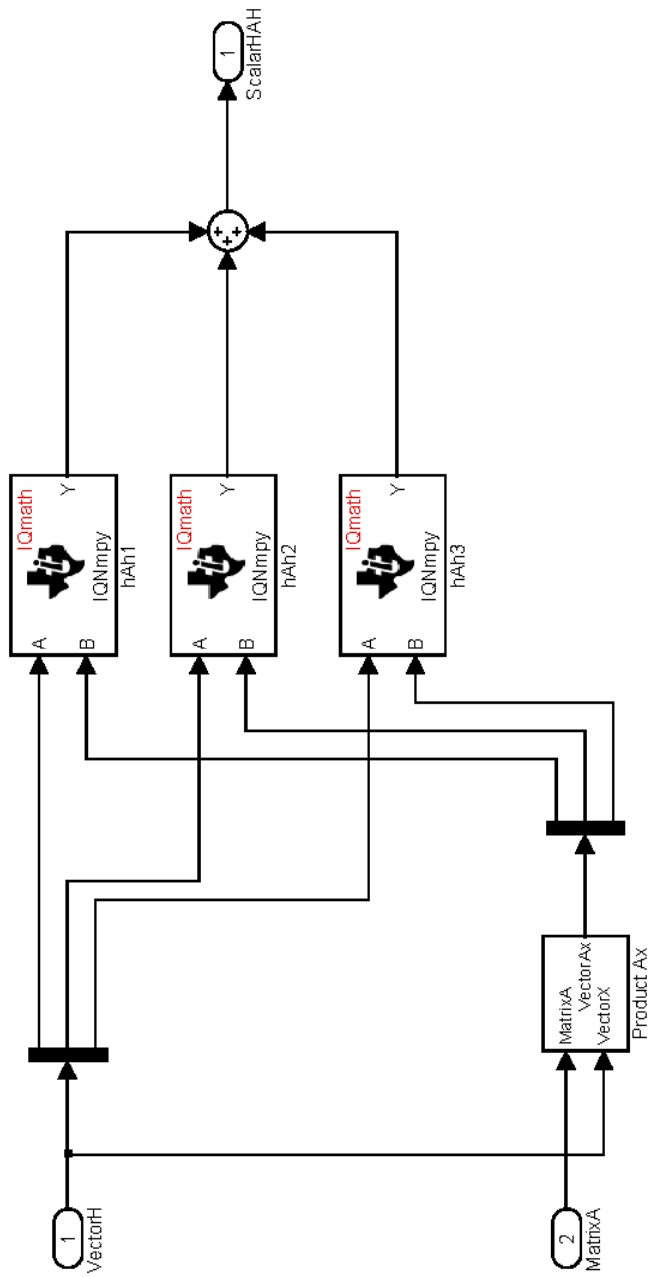
Matrix is stored as a vector, [a11, a12, a21, a22]
 Computes $K=AH^T Z$



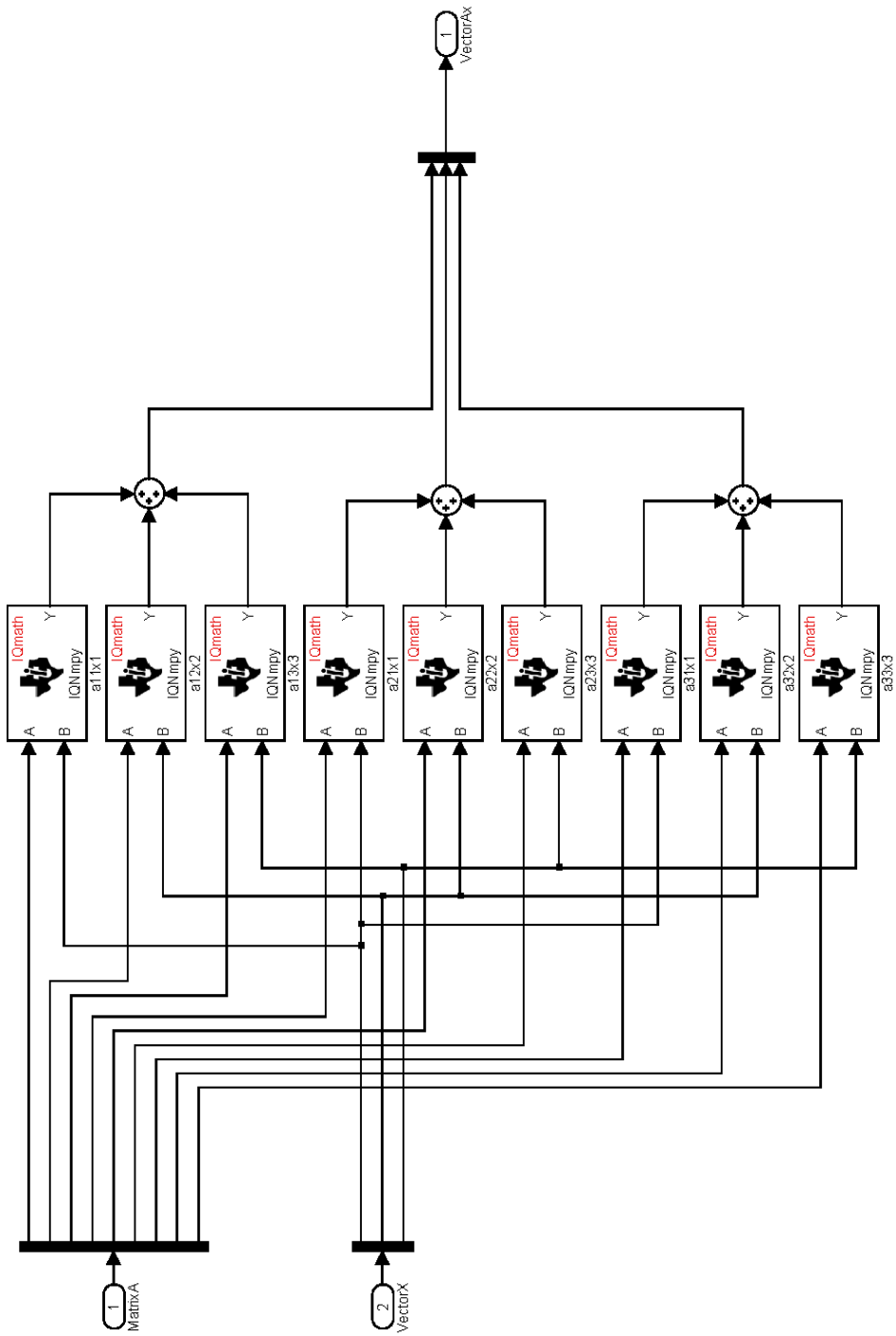
Matrices are stored as vectors. [a11,a12,a13,a21,a22,a23,a31,a32,a33]

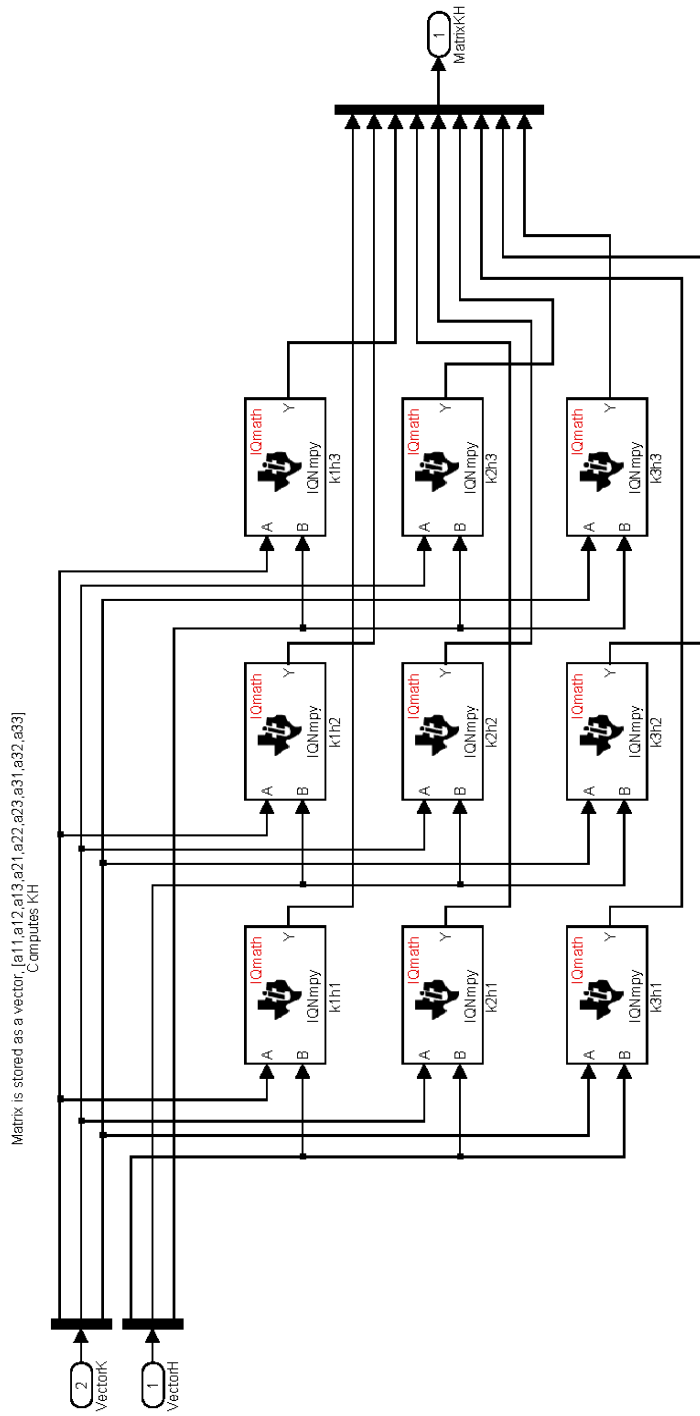


Matrix is stored as a vector
Computes HAH'

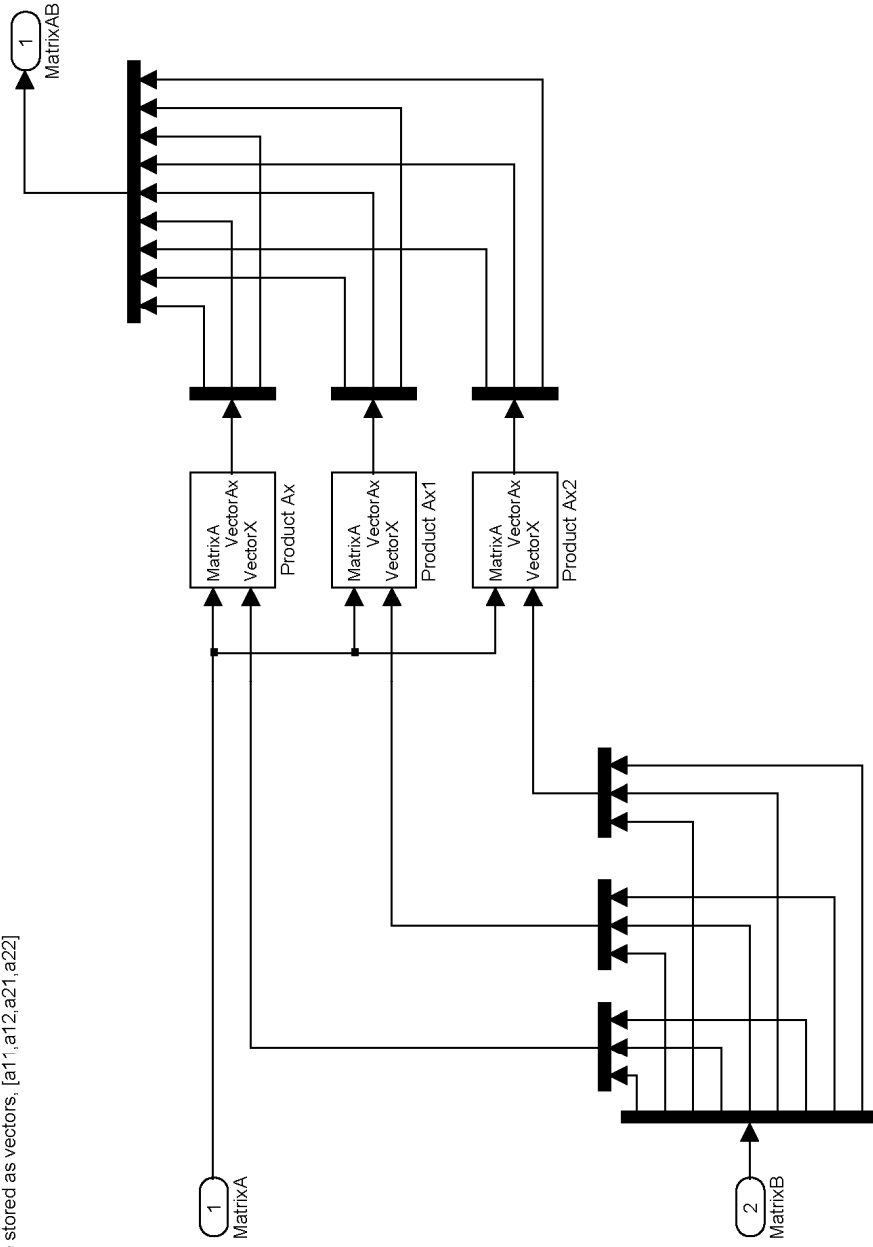


Matrices are stored as vectors. [a11,a12,a13,a21,a22,a23,a31,a32,a33]

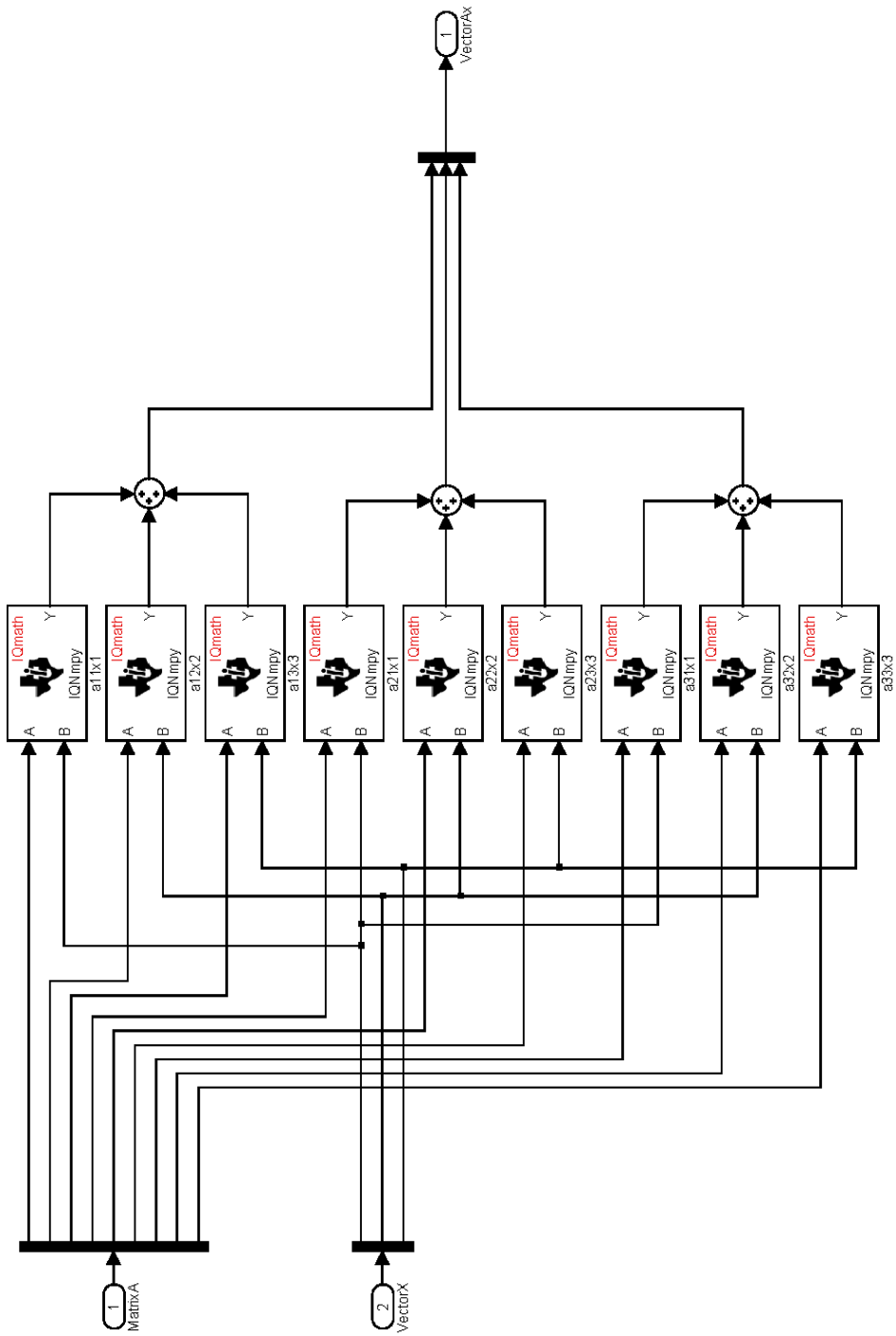




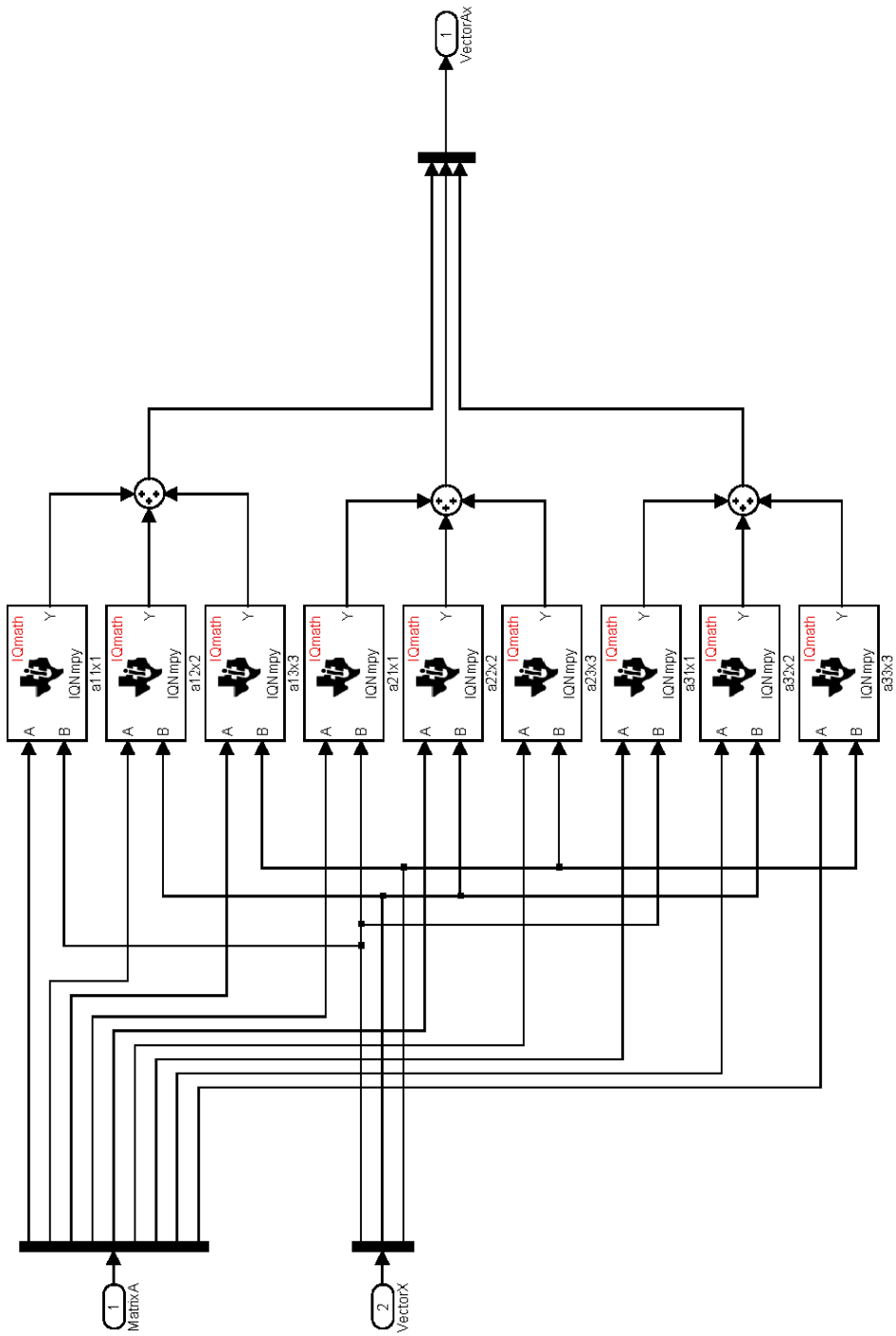
Matrices are stored as vectors, [a11,a12,a21,a22]



Matrices are stored as vectors. [a11,a12,a13,a21,a22,a23,a31,a32,a33]



Matrices are stored as vectors. [a11,a12,a13,a21,a22,a23,a31,a32,a33]



APPENDIX F

C CODE FOR DRCC

The following is “drcc_uiuc_003.c.” This was used for the results shown in Section 5.4.2, along with the schematic shown in Appendix A.

```
// Constant Voltage Fraction + RipCorD Maximum Power Point
Tracker

#include "msp430x14x.h"
#include "drcc_uiuc.h"
#include <stdint.h>

// Functional Overview
//
// At start-up and every 3.3 seconds, the solar panel is open-
circuited by
// disabling switching. Open-circuit voltage Voc is measured to
be used in
// CVF algorithm. Open-circuit "current" is measured to null
offsets in the
// analog signal path.
//
// Next, a CVF algorithm is used. Panel voltage is controlled to
be 0.75*Voc.
// CVF runs for 0.3 seconds.
//
// Finally, a RipCorD algorithm is enabled. The panel voltage is
limited to
// the range [0.6875,0.875]*Voc. This prevents the RipCorD from
running away
// and ensures adequate SNR, adequate ripple. RipCorD runs until
3 seconds
// elapse.
//
// The CVF and RCC algorithms update duty cycle every CYCLE_1
(about 1 ms).
// They also check that the output voltage is below the zener
threshold. This
// prevents the system from driving excessive power into the
zener if the ESI
// shuts down without providing a disable signal.
//
// Modes (g_mode):
// 10: open circuit, switching disabled, sense Voc and Ioc
// 20: CVF, closed-loop control of panel voltage to 0.75*Voc
// 30: sample 1 for RipCorD (external analog switches perform
S&H)
// 40: sample 2 for RipCorD
```

```

// 50: compute new duty cycle for RipCorD
//
// Counters:
// g_count_1: counts PWM cycles within a loop closure (counts to
CYCLE_1)
// g_count_2: counts loop closures (increments every CYCLE_1,
counts to CYCLE_2)

// Function prototypes
__interrupt void Timer_A(void);           // Timer A0 ISR
__interrupt void Timer_A1(void);         // Timer A2 ISR
__interrupt void ADC_ISR(void);         // ADC ISR (used for RCC)
unsigned int read_adc_channel(unsigned int channel); // ADC
sampling
void read_adc_rcc(void);                 // read multiple ADC
channels for RCC
void do_rcc(void);                       // do RCC algorithm using
ADC samples

// Global variable declarations
static unsigned int g_count_1;           // count PWM periods
static unsigned int g_count_2;           // count g_count_1
periods
static unsigned int g_mode;              // modes (listed
above)
static unsigned int g_duty;              // duty cycle
static unsigned int g_isamp1;            // current at
start of PWM sample
static unsigned int g_vsamp1;            // voltage at
start of PWM sample
static unsigned int g_isamp2;            // current at
end of PWM sample
static unsigned int g_vsamp2;            // voltage at
end of PWM sample
static unsigned int g_ioc;                // offset in current
measurement
static unsigned int g_voc;                // open-circuit
voltage
static unsigned int g_vmin;              // minimum panel
voltage (0.625*g_voc)
static unsigned int g_vtarget;           // target panel
voltage for CVF (0.75*g_voc)
static unsigned int g_vmax;              // maximum panel
voltage (0.875*g_voc)
static unsigned int g_ref;                // reference (ripple
offset)
static unsigned int g_vin;                // filtered panel
voltage
static unsigned int g_iin;                // filtered panel
current

```

```

void main(void)
{
    // main() is primarily a setup routine. It initializes the
    // clock, the
    // peripherals, and the global variables g_count_1,
    // g_count_2, and g_mode.
    // At the conclusion, it enters low-power mode so that the
    // core only comes
    // on during interrupt service routines.
    // INPUTS: none
    // OUTPUTS: none
    // GLOBALS: g_duty, g_count_1, g_count_2, g_mode
    (initialize)

    // Set up clock for ~5 MHz
    DCOCTL = (DCO2 | DCO1 | DCO0);

    BCSCTL1 = (XT2OFF | XTS | RSEL2 | RSEL1 | RSEL0);

    BCSCTL2 = 0;

    WDTCTL = WDTPW + WDTCNTCL; // clear running watchdog timer

    // Set up I/O pins
    P1DIR = (Q | TA2_1 | TA2_2);
    P1SEL = Q | TA2_1 | TA2_2; // give peripheral control of
PWM command
    P1OUT = 0; // leave in DCM until things get going
    P2DIR = LED;
    P2OUT = 0xFF;
    P3DIR = 0;
    P4DIR = 0;
    P5DIR = 0;
    P6DIR = 0;
    P6SEL = 0xFF;

    // Set up ADC12 module for multiple sampling, 3.2 us sample
time
    ADC12CTL0 = SHT0_2 | SHT1_2 | REFON | ADC12ON | MSC;
    ADC12CTL1 = SHP | ADC12SSEL_3 | CONSEQ_1 | CSTARTADD_0;
    ADC12MCTL0 = (SREF_1 | ISAMP1 | EOS); // set to read
offset in current

    // Set up PWM module
    g_duty = PWMDUTY;
    TACCTL0 = CCIE;
    // interrupt on every PWM period
    CCR0 = PWMPERIOD;

    TACTL = (TASSEL_2 | MC_1); // Use SMCLK, up mode
    CCR1 = g_duty;
    // CCR1/CCR0 = D

```



```

        g_mode = 20;
        // enable CVF algorithm
        g_duty = PWMDUTY;
        CCR1 = g_duty;
        CCR2 = g_duty;
        g_voc = read_adc_channel(VIN);
        P1OUT &= ~TA2_1;
        g_ioc = read_adc_channel(ISAMP1);

        // panel voltage is later scaled by 16
        g_vmin = (6*g_voc);
        // lower bound is 3/8 of Voc
        g_vtarget = (10*g_voc);           // target is 5/8
of Voc (intentionally low)
        g_vmax = (14*g_voc);
        // upper bound is 7/8 of Voc
        TACCTL1 = OUTMOD_6;
        P2OUT = 0xFF;
    }
}
else if (g_mode == 20)
// CVF algorithm
{
    g_count_1++;
    if (g_count_1 == CYCLE_1)
    {
        g_count_1 = 0;
        g_count_2++;
        l_vpanel = read_adc_channel(VIN) << 4;
        // adjust duty cycle to regulate panel voltage
        if (l_vpanel > g_vtarget)
        {
            g_duty++;
            CCR1 = g_duty;
        }
        else if (l_vpanel < g_vtarget)
        {
            g_duty--;
            CCR1 = g_duty;
        }
        if (g_count_2 == CYCLE_2) // ran CVF long
enough, enable RCC
        {
            g_count_2 = 0;
            g_mode = 30;
        }
    }
}
else if (g_mode == 30)
// idle RCC mode
{
    P2OUT = 0;

```

```

    g_count_1++;
    if (g_count_1 == CYCLE_1)
    {
        g_count_1 = 0;
        g_count_2++;
        if (g_count_2 == CYCLE_2*10) // ran
DRCC for a while, re-initialize
        {
            g_count_2 = 0;
            g_mode = 10;
            TACCTL1 = (OUTMOD_0);
        }
        else // sample power and do DRCC calc
        {
            TACCTL0 = 0;
            // disable Timer A0 interrupt
            g_mode = 40;
            // set up sample 1
            P1SEL &= ~TA2_2;
            P1SEL |= TA2_1;
            if (g_duty < HALFPERIOD)
            {
                CCR2 = g_duty + ((6*(PWMPERIOD -
g_duty))>>4);
            }
            else
            {
                CCR2 = g_duty + ((5*(PWMPERIOD -
g_duty))>>4);
            }
            TACCTL2 = (OUTMOD_0 | OUT);
            TACCTL2 = OUTMOD_5 | CCIE; // enable
other Timer A interrupt
        }
    }
}
else
{
    // only in here if an error occurred; go back to open-
circuit mode 10
    TACCTL1 = OUTMOD_0;
    TACCTL2 = OUTMOD_0;
    g_mode = 10;
    g_count_1 = 0;
    g_count_2 = 0;
}
}

// Timer A2 interrupt service routine
TIMERA1_ISR(Timer_A1)
__interrupt void Timer_A1(void)

```

```

{
    // Timer_A1() is called after the two sampling instants.
Normally, Timer_A
    // is the only interrupt handler active. In modes 40 and
50, Timer_A1 is
    // active instead.
    // INPUTS: none
    // OUTPUTS: none
    // GLOBALS: g_mode (modify), g_duty (read)

if (g_mode == 40)
{
    // sample 1 has completed, so enable sample 2
    g_mode = 50;
    P1SEL &= ~TA2_1;
    P1SEL |= TA2_2;
    if (g_duty > HALFPERIOD)
    {
        CCR2 = ((6*g_duty)>>4);
    }
    else
    {
        CCR2 = ((5*g_duty)>>4);
    }
    TACCTL2 = (OUTMOD_0 | OUT);
    TACCTL2 = (OUTMOD_5 | CCIE);
}
else if (g_mode == 50)
{
    // both samples are complete, so enable ADC and do RCC
    TACCTL2 = OUTMOD_0;
// reset output and disable interrupt
    g_mode = 30;
    ADC12MCTL0 = (ISAMP1);
    ADC12MCTL1 = (VSAMP1);
    ADC12MCTL2 = (ISAMP2);
    ADC12MCTL3 = (VSAMP2);
    ADC12MCTL4 = (REFERENCE);
    ADC12MCTL5 = (IIN);
    ADC12MCTL6 = (VIN | EOS);
    ADC12IE = BIT3;
    ADC12CTL0 |= (ENC | ADC12SC);
}
else
{
    // only in here in the event of an error, go back to
open circuit
    TACCTL0 = CCIE;
    TACCTL1 = OUTMOD_0;
    TACCTL2 = OUTMOD_0;
    g_mode = 10;
}
}

```

```

}

// Sample ADC12 channel
unsigned int read_adc_channel(unsigned int channel)
{
    // read_adc_channel(channel) samples ADC12 channel.
    // Most of ADC setup is in main().
    // INPUTS: integer of channel to read
    // OUTPUTS: integer representing ADC result
    // GLOBALS: none

    unsigned int l_temp = 0;

    ADC12MCTL0 = (channel | EOS);           // select
channel, use ref=AVCC
    ADC12CTL0 |= (ENC | ADC12SC);          // start sample
    while (ADC12CTL0 & ADC12SC);          // wait for
sample to complete
    l_temp = ADC12MEM0;
    ADC12CTL0 &= ~ENC;
    // disable ADC12 module

    return l_temp;
}

// ADC12 interrupt service routine
ADC12_ISR(ADC_ISR)
__interrupt void ADC_ISR(void)
{
    // ADC_ISR executes whenever the ADC is done converting
current, voltage
    // Results are in ADC registers, to be moved to globals.
At the end, calls
    // do_rcc to actually do the DRCC algorithm, then goes back
to normal mode 30.
    // INPUTS: none
    // OUTPUTS: none
    // GLOBALS: g_isamp1, g_vsamp1, g_isamp2, g_vsamp2 (write)

    ADC12IE = 0;
    ADC12CTL0 &= ~ENC;

    g_isamp1 = ADC12MEM0;
    g_vsamp1 = ADC12MEM1;
    g_isamp2 = ADC12MEM2;
    g_vsamp2 = ADC12MEM3;
    g_ref = ADC12MEM4;
    g_iin = ADC12MEM5;
    g_vin = ADC12MEM6;
    do_rcc();
    TACCTL0 = CCIE;
    // re-enable Timer A0 interrupt

```

```

}

// Evaluate power at two points in cycle, adjust duty cycle
void do_rcc(void)
{
    // do_rcc uses globals to determine whether to increase or
    // decrease duty.
    // INPUTS: none
    // OUTPUTS: none
    // GLOBALS: g_(x)samp(y) (read), g_duty (modify)

    unsigned long int l_power1, l_power2;
    unsigned int l_isampos1, l_isampos2;           //
isamp1 and isamp2 less offset
    unsigned int l_vintot1, l_vintot2;
    // total input voltage

    // ac current has a gain of 32
    l_isampos1 = (g_iin << 4) + (g_isamp1 >> 1) - (g_ref >> 1);
    l_isampos2 = (g_iin << 4) + (g_isamp2 >> 1) - (g_ref >> 1);

    l_vintot1 = (g_vin << 4) + (g_vsamp1 << 2) + (g_vsamp1 >>
1) + (g_vsamp1 >> 2) + (g_vsamp1 >> 4);
    l_vintot1 -= (g_ref << 2) + (g_ref >> 1) + (g_ref >> 2) +
(g_ref >> 4);
    l_vintot2 = (g_vin << 4) + (g_vsamp2 << 2) + (g_vsamp2 >>
1) + (g_vsamp2 >> 2) + (g_vsamp2 >> 4);
    l_vintot2 -= (g_ref << 2) + (g_ref >> 1) + (g_ref >> 2) +
(g_ref >> 4);

    l_power1 = ((long int) l_vintot1) * ((long int)
l_isampos1);
    l_power2 = ((long int) l_vintot2) * ((long int)
l_isampos2);

    // changed polarity of power comparison to match new
    // sampling times (08-22-06)
    // first do DRCC: change duty in response to power
    // difference; also enforce
    // voltage limits as determined from CVF algorithm.
    if ((l_power1 < l_power2) || ((g_vin << 4) < g_vmin))
    {
        g_duty--;
    }
    else if ((l_power1 > l_power2) || ((g_vin << 4) > g_vmax))
    {
        g_duty++;
    }

    // next enforce duty cycle limits
    if (g_duty < MINDUTY)
    {

```

```

        g_duty = MINDUTY;
    }
    else if (g_duty > MAXDUTY)
    {
        g_duty = MAXDUTY;
    }

    // now g_duty is properly computed and limited, so use it
    CCR1 = g_duty;
    return;
}

```

The following is “drcc_uiuc.h.”

```

// Constant Voltage Fraction + RCC Maximum Power Point Tracker

// Inclusion guard
#ifndef _RIPCORD_H_INCLUDED_
#define _RIPCORD_H_INCLUDED_

// define timing parameters: PWM period, PWM duty cycle, feedback
loop, Voc loop

#define PWMPERIOD 200 // CCR0 setting to determine PWM
period
#define HALFPERIOD 100 // half of PWMPERIOD, used for
threshold in RCC

// sampling process
#define PWMDUTY 30 // CCR1 setting to
determine initial duty cycle

#define CYCLE_1 20 // Number of PWM cycles for
low-level monitoring
#define CYCLE_2 300 // Number of low-level
cycles in high-level cycle
#define MINDUTY 10 // Minimum duty cycle
is MINDUTY / PWMPERIOD

#define MAXDUTY 175 // Maximum duty cycle
is MAXDUTY / PWMPERIOD
// define CVF parameters
// need to recalculate MAXOUTVOLT
#define MAXOUTVOLT 2013 // limit on output

// for 22k1, 200k divider, 2.5 V ref, 12 bit ADC
// Nadc = Vdcbus * 163
// 2013 => 12.35 V (min Vz for 1N5350)

```

```

// Define all the pins (names according to schematic)

// ADC12
#define IIN                INCH_0           // filtered
panel current (NEW 02 Apr 07)
#define VIN                INCH_1           // filtered
input voltage
#define ISAMP1             INCH_2           // current sampled by
SAMPLE1
#define REFERENCE         INCH_3           // 1.235V reference (offset
on VSAMPx)
#define VSAMP2            INCH_4           // voltage sampled by
SAMPLE2
#define VSAMP1            INCH_5           // voltage sampled by
SAMPLE1
#define ISAMP2            INCH_6           // current sampled by
SAMPLE2

#define LED                BIT0            // LED output
(low -> LED on) : Port 2
#define Q                  BIT2            // PWM command
(high -> FET on) : Port 1
#define TA2_1              BIT3            // timer A2 output #1
: Port 1
#define TA2_2              BIT7            // timer A2 output #2
: Port 1

// End inclusion guard
#endif

```

AUTHOR'S BIOGRAPHY

Jonathan W. Kimball was born in McKeesport, Pennsylvania, in 1973 and grew up in suburban Pittsburgh. He received the B.S. degree in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, Pennsylvania, in 1994 and the M.S. degree in electrical engineering from the University of Illinois at Urbana-Champaign in 1996.

He worked for Motorola, Phoenix, Arizona, designing IGBT modules for industrial applications. He then joined Baldor Electric, Fort Smith, Arkansas, where he designed industrial adjustable speed drives ranging 1–150 hp. In 2003, he returned to the University of Illinois as a Research Engineer (currently a Senior Research Engineer). He is also a founder and Vice President of Engineering for SmartSpark Energy Systems, Inc., Champaign, Illinois. Following completion of his Ph.D., he will be an assistant professor at Missouri University of Science and Technology (Missouri S&T, formerly University of Missouri-Rolla).

Mr. Kimball is a member of Eta Kappa Nu, Tau Beta Pi, and Phi Kappa Phi. He is a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE). He is a licensed Professional Engineer in the State of Illinois.