

APPLICATION OF NONLINEAR CONTROL TECHNIQUES IN LOW  
VOLTAGE DC-DC CONVERTERS

BY

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B.S., Carnegie Mellon University, 1994

THESIS

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**PAP-TR-96-6  
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**Power Affiliates Program  
Department of Electrical and Computer Engineering  
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Urbana, Illinois 61801**

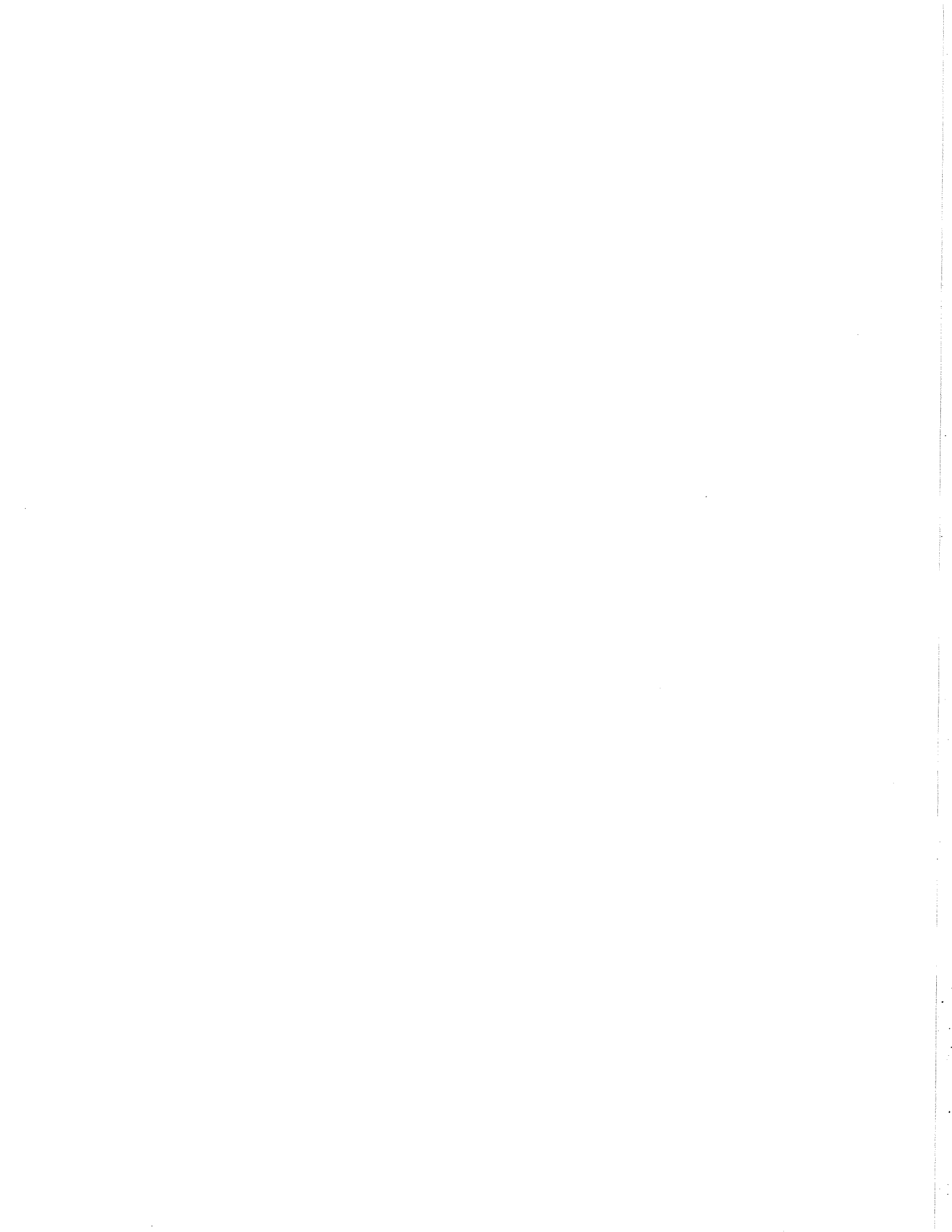
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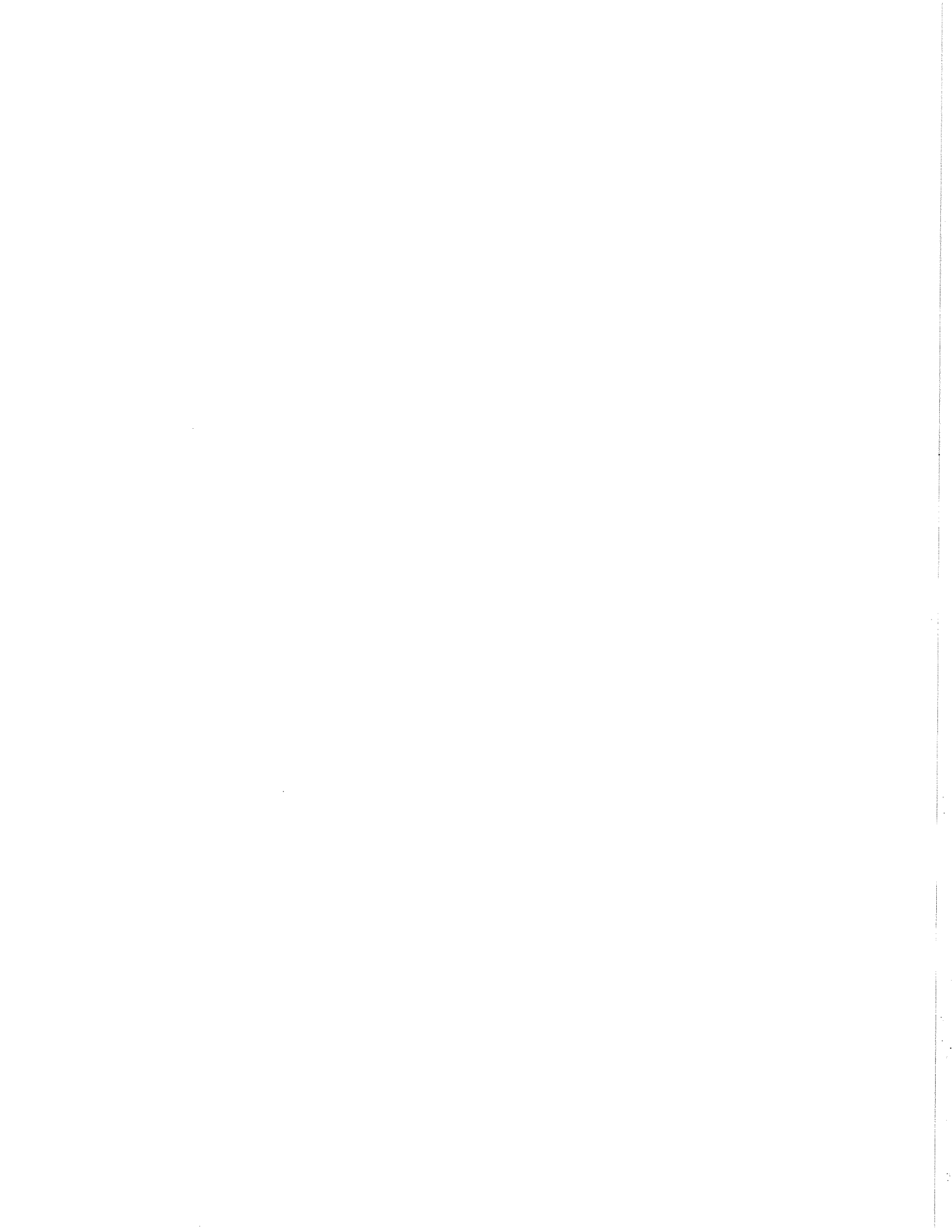
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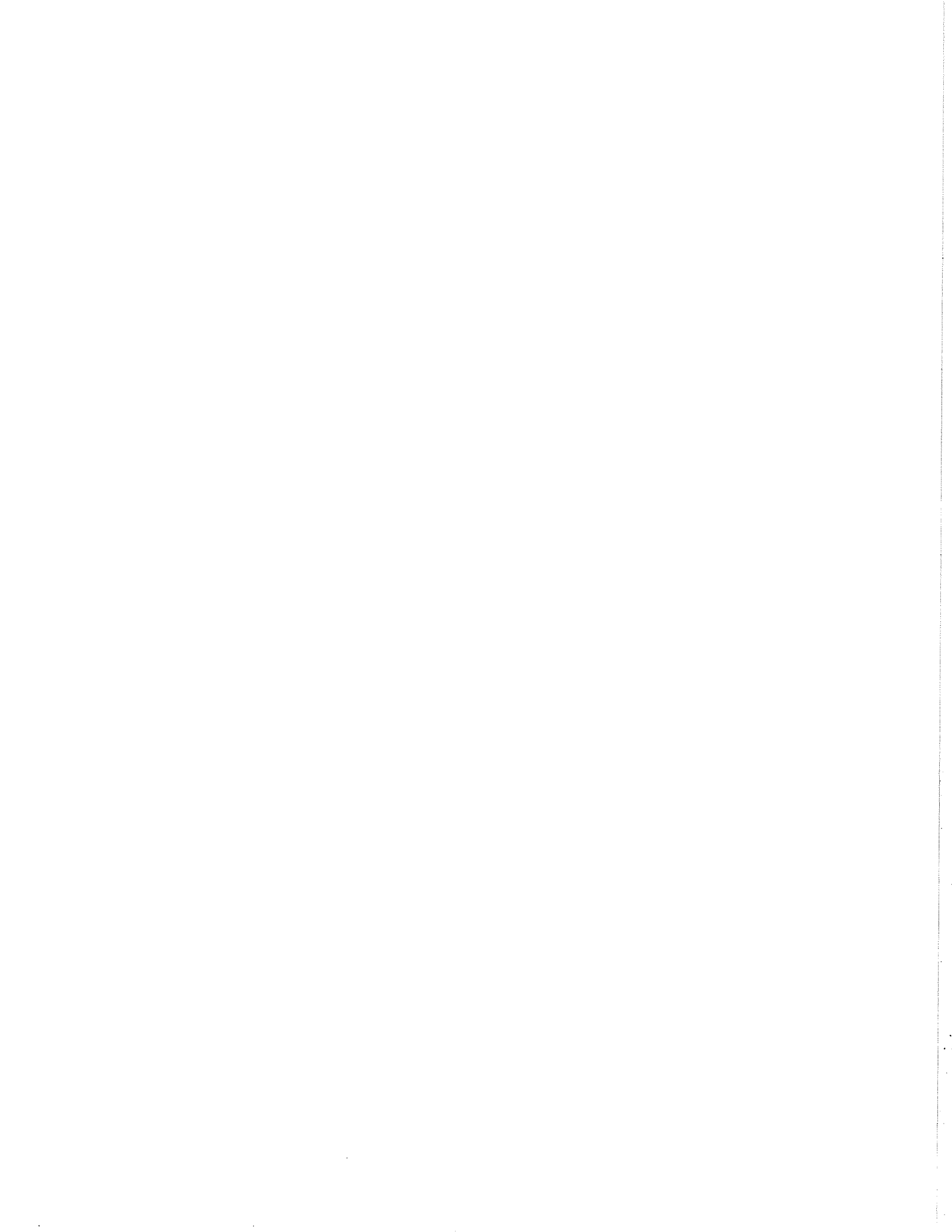
## FOREWARD

This technical report is a reprint of the thesis written by Jonathan William Kimball as partial fulfillment of the requirements for the degree of Master of Science in Electrical and Computer Engineering at the University of Illinois.

Philip T. Krein

Thesis Advisor

May 1996



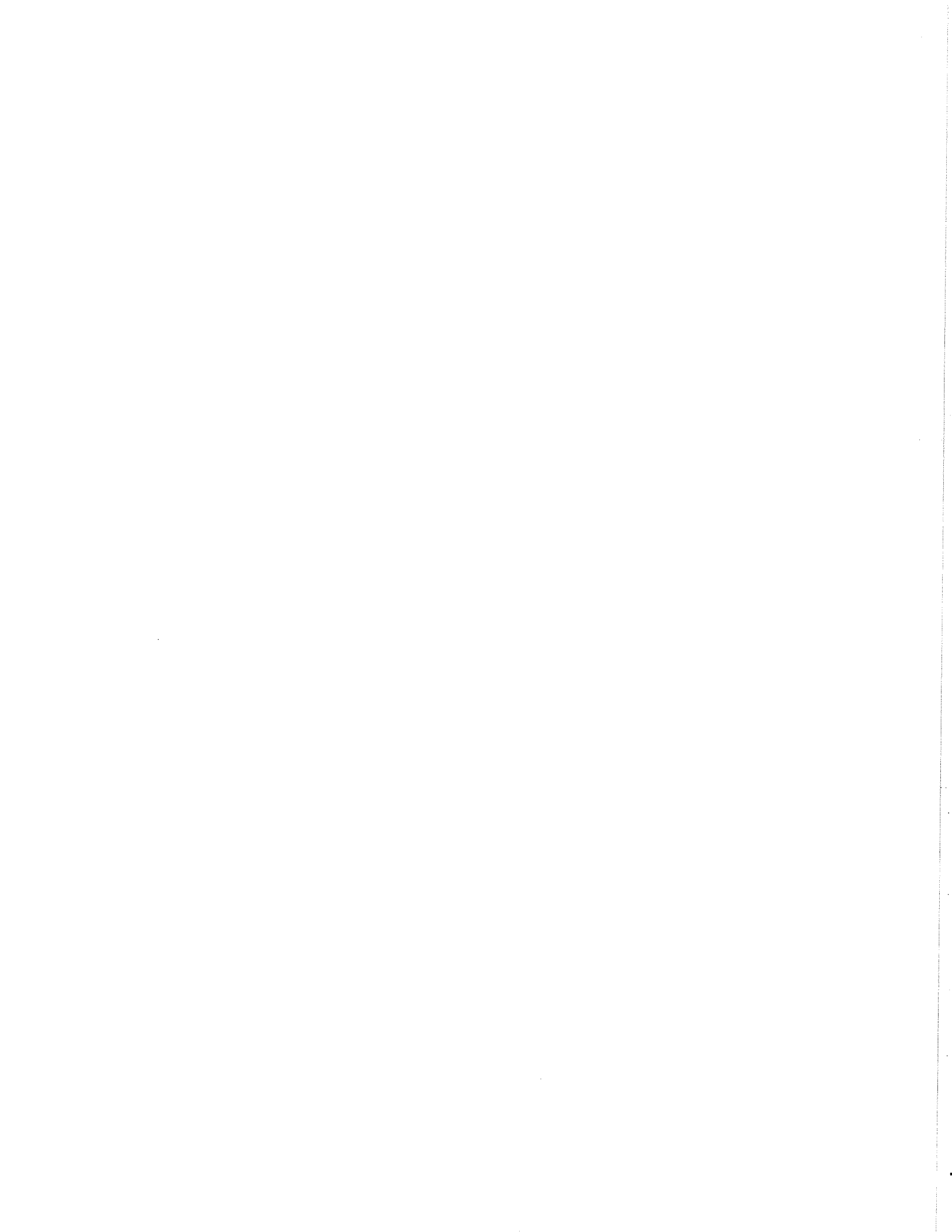
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## CHAPTER 1 INTRODUCTION

Each generation of digital electronics calls for a lower voltage power supply. Until the advent of portable computers, 5 V logic dominated the microprocessor world. Now, even desktop computers use 3.3 V logic, and 2.5 V microprocessors are available. We can expect 1 V logic in the near future, pushing the limits of current power electronics technology.

Power electronic circuits can be classified into two basic categories, linear regulators and switching power converters. Linear regulators closely resemble traditional analog circuits. A linear regulator can be designed with essentially no output ripple; unfortunately, this comes at the cost of efficiency. Switching power converters achieve dc-dc conversion by using transistors or other semiconductor devices as switches, along with one or more energy storage elements such as inductors and capacitors. The switching action introduces ripple in the output of the converter, but can in principle achieve arbitrarily high efficiency, depending only on the parasitic resistances of the components used and losses due to switching.

At low output voltages, the ripple introduced by switching converters greatly affects the design. While a 12 V  $\pm 1\%$  output allows 120 mV of ripple, a 1 V  $\pm 1\%$  output tolerates only 10 mV of ripple. Typical designs rely on large inductor and large capacitors as well as high switching frequency to achieve this extreme goal, although there

are practical limits to both. Devices with high inductance or capacitance are physically large, reducing possible performance in space-critical or weight-critical applications. At high frequencies (hundreds of kHz and up), parasitic inductance and capacitance can severely reduce the expected performance of a design. In order to effectively use conventional methods at low voltages, surface mount devices, application-specific ICs, or more exotic packaging like multi-chip modules are necessary.

Efficiency becomes a serious issue at low voltages. With output voltages of 5 V and up, a diode (either standard p-n junction or Schottky) can be used as one switch. At low voltages, the forward drop inherent to any diode can dominate the losses in the converter. At moderate current levels, a typical Schottky has about a 0.5 V forward drop; for a 1 V output, this corresponds to 33% loss while the diode is conducting. The most commonly proposed option is to use a synchronous rectifier, which consists of a MOSFET and some control circuitry to emulate the function of a diode. For commercial products, the control is often designed to be very simple, rather than being optimally efficient.

One option for achieving low ripple is to use linear regulators, noted for good stability and low noise. They are not, however, noted for good efficiency; the theoretical maximum is given as  $V_{out}/V_{in}$ , the ratio of output voltage to input voltage. While this may be a feasible solution for desktop computers, it is certainly not the best option for portable computers.

The alternative to using linear regulators is to develop advanced switching converters and control techniques. This thesis covers both ripple and efficiency issues:

first a method for actively reducing ripple is extended and analyzed (Chapter 2), then a method for optimizing the efficiency of a synchronous rectifier is developed (Chapter 3). Finally, two power converters are built, one (2 V at 1 W) as a test-bed for various concepts, the other as a sample of what future power converters might resemble (1 V at 25 W). Results for both will be discussed in Chapter 4.

### **1.1 Requirements for Modern Power Converters**

Low output voltage levels require output voltage ripple to be much smaller on an absolute scale. For example, a 5 V output with  $\pm 1\%$  ripple allows  $\pm 50$  mV ripple, while a 1 V output would only allow  $\pm 10$  mV ripple. If the current level remains constant and the design techniques are not enhanced, the output capacitance would have to be five times as large. Another solution is required if, as is usually the case, cost and space constrain the overall design.

Dynamic performance constrains any technique for achieving power conversion goals. As voltages drop and power remains constant, rated load impedance for the converter drops. A power converter rated for 5 V at 10 W has a rated load impedance of  $2.5 \Omega$ ; one rated for 1 V at 10 W has a rated load impedance of only  $0.1 \Omega$ . Any passive filter designed to reduce ripple must have a total impedance much lower than the load impedance at the operating frequency. If a filter with impedance much less than  $0.1 \Omega$  could be built, it would compromise dynamic response, as mentioned in [1] and [2]. Active filters must be considered as an alternative solution.

Slew rate also becomes a significant issue. During start-up and other significant changes in operating conditions, microprocessors can swing as much as half of the maximum rated current in one or two clock cycles. Total lead inductance can, at best, be reduced to 1 nH, and near-future microprocessors can be expected to operate at up to 500 MHz. For a 10 A maximum load, a one-cycle 50% swing means 2500 A/ $\mu$ s slew rate. Lead inductance alone results in a 2.5 V spike, clearly unacceptable for a microprocessor. Bulk capacitance on the chip itself improves the situation, but active techniques to enhance performance external to the chip could be cost-effective. In order to meet the dynamic performance goals of advanced power converters, control methods have to be developed or enhanced.

## **1.2 Conventional Techniques**

Many of the problems discussed in Section 1.1 are relevant to the design of power converters at 3.3 V, and so have been addressed to some degree even in commercial products. Improvements have to be made in order to handle lower voltage outputs.

Despite the drawbacks, passive filters are often used to reduce output ripple. One alternative is to use a coupled inductor configured as a flyback converter to generate another output from the ripple [3]. In certain cases the auxiliary output is useful or even necessary. If not, then the extra output is either lossy or ineffective at reducing ripple, or both. Active filters have also been suggested; the specifics and characteristics of these approaches are detailed in Chapter 2.

A known technique for improving efficiency at low voltage levels is synchronous rectification. As described above, the (Schottky) rectifier found in standard buck converters is replaced with a controlled MOSFET; a good overview of the various other applications of synchronous rectifiers may be found in [4]. The difficulty lies in generating the appropriate gate signals. Generally, the two gate signals are nearly complementary, with some dead-time inserted when both gates are held low. This dead-time ensures that at most one device is fully on at any given time. The anti-parallel body diode of typical power MOSFETs guarantees a conduction path for the inductor current. Because this diode is relatively lossy, a Schottky rectifier is sometimes put in parallel with the MOSFET; in other words, the Schottky rectifier is augmented by a MOSFET synchronous rectifier, not replaced.

### **1.3 Summary of New Techniques**

A feed-forward active filter is described in detail in Chapter 2. The technique was proposed in [5]; here, we explore the limits of useful operation. Many times the frequency limitations can be traced to the operational amplifiers used to generate the compensation, but there are additional effects fundamental to the filter even using idealized operational amplifiers. These limitations and their net effect are examined. The feed-forward technique is also compared to a feedback technique, to explore stability and implementation issues.

Chapter 3 describes a new method for generating gate signals for a converter using a synchronous rectifier. This is an extension of the general correlation-based technique described in [5]-[7] to switching function signals; theoretical development is given, along with experimental results. The new technique dynamically minimizes input current, guaranteeing precise timing to allow for proper commutation of the inductor current.

Two converters, described in Chapter 4, have been constructed to show the feasibility of the above methods. Both converters use the buck topology. The first is a 5 V input, 2 V output 1 W converter, which was used as a test bed for developing the techniques and demonstrating their compatibility without interference. The second is a 5 V input, 1 V output 25 W converter. The higher power level makes this converter a practical example of potential near-future power converters. As digital technology develops, such a power converter will soon be needed, and the control techniques proposed are viable options for achieving the performance required.

## CHAPTER 2 FEED-FORWARD ACTIVE FILTER

Output ripple is a serious concern in low-voltage power converters. For a variety of reasons, passive filtering is inadequate for attaining the desired specifications for many applications. Here, a feed-forward method for active filtering of ripple in a buck converter is analyzed and compared to a more conventional feedback technique.

### 2.1 Theory of Operation

Most output filtering schemes do not consider the basic source of voltage ripple in a buck converter: inductor current ripple. For reference, a circuit diagram for a conventional buck converter is shown in Figure 3.1, page 28. In many space-sensitive applications, the size of the inductor ( $L$ ) is reduced, resulting in larger current ripple; the difference is made up with a larger output capacitor ( $C$ ). To be effective, the  $LC$  pair must have a high  $Q$  factor, so that any equivalent series resistance (ESR) in either element becomes significant. In fact, ESR ultimately limits the designed performance of the filter. An alternative is to include an active filter to cancel the inductor current ripple.

Similar active filters were proposed in [1] and [8]-[10] to correct for input current ripple. Most of the previous work is applicable to 60 Hz systems, changing the basic design requirements for the magnetic elements. Here, the technique is modified and improved to correct output current and voltage ripple at high frequencies, with results given for 200 kHz systems.

While other filter elements are often present, a single inductor generally dominates the current ripple. Assuming the inductor always operates as a perfect lossless linear element, the current can be found easily from:

$$i_L = \frac{1}{L} \int v_L dt \quad (2.1)$$

where  $v_L$  is the differential voltage across the inductor and  $i_L$  is the conducted current. So, without a current shunt or other current-measuring device, the current can easily be found from terminal voltages with an operational amplifier (op amp) circuit. The estimate can be improved by including the ESR of the inductor. With some series resistance, the inductor behaves like a single-pole system, with the pole at  $\omega = R/L$ . An op amp circuit with a single pole at the same radian frequency exactly duplicates the frequency characteristics of a linear inductor. The feed-forward method aims to eliminate the ac portion of the inductor current, so the output of the integrator or single-pole filter can be ac-coupled to the rest of the system.

The filter uses the signal proportional to inductor current ripple to generate a compensation current. Operation at this point, as described in [5], uses a voltage-to-current circuit to inject a current into the power converter exactly  $180^\circ$  out of phase with the inductor current, resulting in a net ac current of zero. To implement this with standard analog parts, the current is injected into the primary side of a transformer, the secondary coil of which is ac-coupled to the output of the power converter. A

standard op amp, which is generally limited to approximately 100 mA of output current, can supply a few amps of compensation current to the power converter through a properly designed transformer.

This analysis assumes that the inductance is a known time-invariant quantity. In actual operation, there is uncertainty in the inductance value used. Nonlinear effects can be significant, and temperature and other factors can change the effective inductance over time. As a result, an auto-tuning algorithm has been developed to compensate for these factors. The general technique proposed in [5] will be discussed in detail in Chapter 3; here follows a derivation of this specific algorithm.

Assuming the inductor can be approximated as linear over short time scales, the compensating current is given as

$$i_{comp} = -k \int \frac{v_L}{L_{est}} dt \quad (2.2)$$

where optimal compensation occurs at  $k = L_{est}/L$ . This allows the gain to be tuned to match the actual inductance. The voltage ripple may then be expressed as

$$v_{ripple} = Z_{out} \left( 1 - k \frac{L}{L_{est}} \right) i_{nocomp} \quad (2.3)$$

where  $Z_{out}$  is the effective impedance seen at the output, including any post-compensation filtering, and  $i_{nocomp}$  is the current ripple normally seen at the output in the absence of any

active filter. Define a correlation function used to adjust  $k$  as

$$c_P = v_{ripple} \int \frac{v_L}{L_{est}} dt \quad (2.4)$$
$$\frac{dk}{dt} = \frac{c_P}{T}$$

Thus  $k$  is adjusted using integral control. Results shown in [5] demonstrate the effectiveness of this technique for minimizing output voltage ripple under varying loads. The method should be similarly stable for other variations, such as temperature.

## 2.2 Frequency Characteristics

The frequency range over which the technique is usable remains undetermined. As frequency increases, parasitic elements affect operation, nonlinearities in the magnetics become more significant, and the power converter becomes more sensitive to timing variations. The first issue to address is the linear circuit model for the current transformer.

Figure 2.1 shows the (nearly) full equivalent circuit for a transformer, including winding capacitance and parasitic resistances. The figure also shows a damper resistor  $R_\phi$  necessary to reduce high-frequency oscillations. The element marked 'X' is an equivalent ideal transformer.

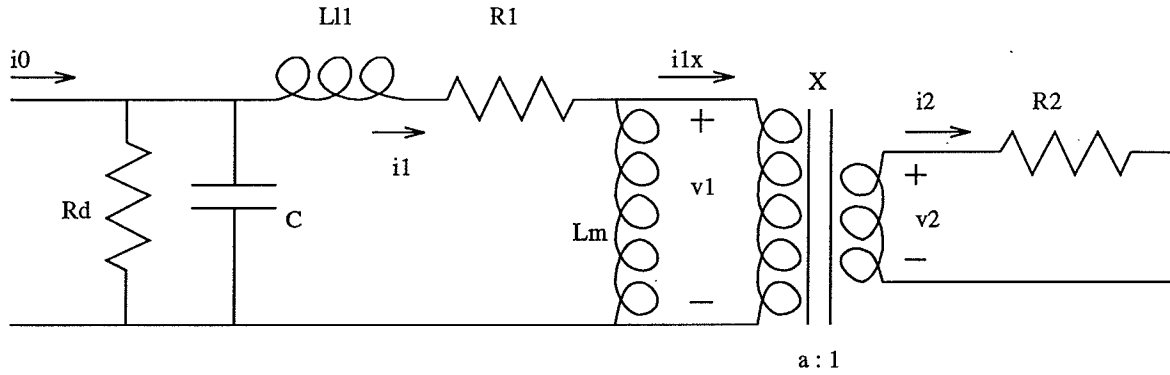


Figure 2.1: Transformer Model

To begin analyzing the circuit, note that  $i_2 = a i_{1x}$  and  $v_1 = a v_2$ , where  $a$  is the turns ratio of the transformer. Additionally,  $v_2 = i_2 R_2$ . Using the variables defined in Figure 2.1, the following relationships hold:

$$\begin{aligned}
 v_1 &= a^2 i_{1x} R_2 \\
 i_1 &= i_{1x} \left( 1 + a^2 \frac{R_2}{sL_m} \right) \\
 v_0 &= v_1 + i_1 (R_1 + sL_1) \\
 i_0 &= i_1 + v_0 \left( \frac{1}{R_d} + sC \right)
 \end{aligned} \tag{2.5}$$

With some simplification, the transfer function  $H(s) = i_2/i_0$  becomes

$$H(s) = \frac{s (aL_m R_2)}{d_0 + s d_1 + s^2 d_2 + s^3 d_3} \tag{2.6}$$

with coefficients given by

$$\begin{aligned}
d_0 &= (1 + a^2 R_2 (R_1 + R_d)) \\
d_1 &= (L_m R_1 + L_{l1} R_2 + a^2 R_1 R_2 R_d C + a^2 L_m R_2) \\
d_2 &= (L_m L_{l1} + L_m C R_1 R_d + a^2 L_{l1} C R_2 R_d + a^2 L_m C R_2 R_d) \\
d_3 &= (C L_{l1} L_m R_d)
\end{aligned} \tag{2.7}$$

The capacitance term can be neglected in many transformers. In this application, however, the capacitance becomes a significant term, even if only tens of picofarads. One transformer used in some experiments described in Section 2.4 has an  $L_m C$  resonant frequency around 250 kHz, corresponding to a self-capacitance of 12 pF. For adequate compensation, the frequency response is relevant up to 2 MHz or higher in order to capture all the harmonics associated with the triangle wave current. Leakage inductance can also dramatically alter the frequency response. As explored below, for some range of frequencies, the three poles combine to generate essentially a fixed time delay. This delay ultimately limits the effectiveness of the filtering technique.

A full design was carried through for the following system, a transformer constructed on a ferrite toroid:

$$\begin{aligned}
L_m &= 72.55 \text{ mH} & L_{l1} &= 618 \text{ } \mu\text{H} \\
R_1 &= 36 \text{ } \Omega & R_2 &= 8 \text{ m}\Omega \\
C &= 15.6 \text{ pF} & R_d &= 1 \text{ k}\Omega
\end{aligned}$$

The load is defined as a 40 m $\Omega$ /660  $\mu$ F parallel combination, appropriate to a 1 V, 25 W output stage. If the basic system described above is used, there is no attenuation, only a

phase shift. The underlying problem is leakage inductance in the current transformer. Even at less than 1% of the magnetizing inductance, leakage is large enough that it adds a pole below the frequency of interest, so that the transfer function is no longer flat. The insertion of a compensator stage shows some promise in simulation. To ensure stability and noise immunity, the compensator should have a proper transfer function. Good results are seen with:

$$G(s) = k \frac{s + p_1}{s + 5.4 \times 10^6} \quad (2.8)$$

$$H'(s) = H(s)G(s)$$

where  $p_1$  corresponds to the offending pole created by the leakage inductance; for the transformer being used,  $p_1 = 6.74 \times 10^4$  rad/s. The gain  $k$  can be chosen adaptively to minimize output voltage ripple; it corresponds to maximum (high-frequency) gain. For the simulation,  $k$  was found manually to be 3.35, which attenuates output ripple by 9.07 dB.

For simple comparisons, the transfer function  $H'(s)$  defined in Equations (2.6-2.8) can be approximated as a pure time delay  $\delta t$ . As shown in Figure 2.2, this reduces the ripple current to a trapezoidal wave with a peak given by

$$\frac{I_{ro}}{I_o} = 4 \frac{\delta t}{T} \quad (2.9)$$

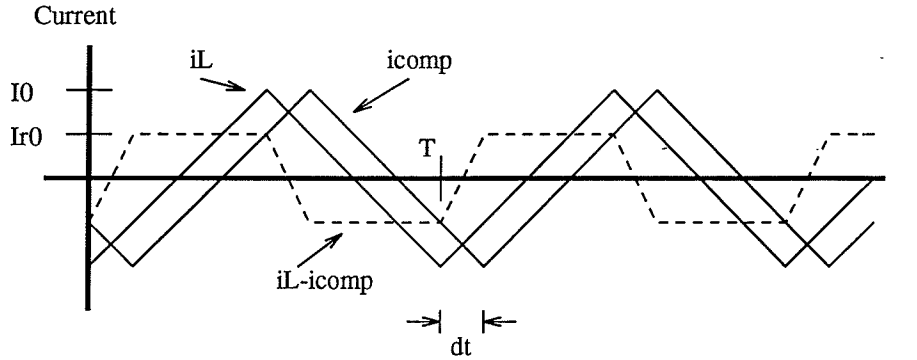


Figure 2.2: Comparison of  $i_L$  and  $i_{comp}$

Output ripple voltage is essentially ripple current multiplied by output impedance, so reduction in either has the same net effect. For a nominal output impedance of  $Z(s)$ , the effective output impedance is reduced by compensation to

$$\frac{\bar{v}_o}{\bar{i}_L} = 4 \frac{\delta t}{T} Z(s) \quad (2.10)$$

For the transformer discussed in Section 2.4,  $\delta t \approx 300$  ns, so at 200 kHz switching, the effective impedance is only 24% of  $Z(s)$ . Compensation techniques can reduce  $\delta t$  to about 70 ns, decreasing the effective impedance to 5.6% of  $Z(s)$ . If the output capacitor dominates the load impedance at the frequency of interest, then using this transformer in a feed-forward system is equivalent to increasing output capacitance by a factor of 18. Large capacitances are often not feasible for a given application, because of size, cost, and ESR constraints. The feed-forward filter could be competitive in such a system, with adequate high-frequency magnetic design.

### 2.3 Feedback Compensator Analysis

The feed-forward method, while highly effective, has certain limitations. The transformer used for injecting current imposes some phase delay or time delay, which cannot be accounted for in real-time. Although the goal is to minimize output ripple, the actual output voltage is only used to adjust a gain, with slow dynamics. Given these limitations, one might consider a more traditional feedback compensator.

Rather than sensing the inductor voltage and using it to generate the compensation current, one could sense the output voltage directly, as discussed in [2]. The compensation current signal could be generated by a proportional-integral (PI) loop as

$$i_{comp} = \left( K_p + \frac{K_i}{s} \right) H(s) (v_{out} - V_{REF}) = B(s) H(s) \tilde{v}_{out} \quad (2.11)$$

where  $H(s)$  is the transfer function of the transformer as defined in (2.6) and (2.7) and  $V_{REF}$  is the desired dc output voltage. The output voltage ripple can be found by looking at ripple current into the output impedance. For simplicity, assume the output impedance  $Z(s)$  is some load resistor  $R_L$  in parallel with a filter capacitance  $C_L$ :

$$\tilde{v}_{out} = (\tilde{i}_L - i_{comp}) \left( R_L \parallel \frac{1}{sC_L} \right) = (\tilde{i}_L - i_{comp}) Z(s) \quad (2.12)$$

Substituting the control law for  $i_{comp}$ , the effective output impedance is

$$\frac{\bar{v}_{out}}{\bar{i}_L} = \frac{Z(s)}{1 + \left(K_p + \frac{K_i}{s}\right)H(s)Z(s)} \quad (2.13)$$

The transfer function in (2.11) is equivalent to the system shown in Figure 2.3.

A full design has been carried through for the same system considered in the previous section. Using MATLAB, optimal design techniques are straightforward, particularly the linear quadratic regulator (LQR). LQR design is of the form  $u = -Kx$ , where  $u$  is the input and  $x$  is a vector of the states. In the current design, only the state corresponding to output voltage ripple is penalized; the results show that only this state contributes much to the feedback, so a nearly equivalent formulation is  $u = -K_p V_o$ . In

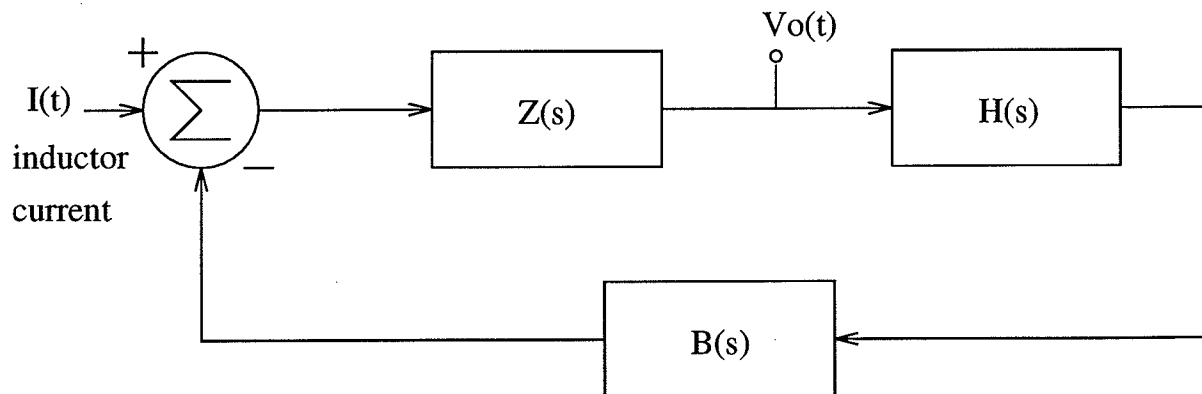


Figure 2.3: Proposed Feedback System

order to achieve 9.06 dB attenuation,  $K_p = 4.84 \times 10^6$  (134 dB). If  $K_p$  is constrained to be, for example,  $1 \times 10^4$  (80 dB), there is essentially no attenuation (0.006 dB).

Surprisingly, integral gain makes the system unstable. Using a perfect current transformer, any choice of  $K_p$  and  $K_i$  results in a stable system. The time-delay effect of the real transformer results in enough phase delay to make any appreciable integral gain destabilizing. Root loci are shown in Figures 2.4 and 2.5 for purely integral gain ( $K_p = 0$ ); Figure 2.5 is a magnification of the region near the origin. The upper and lower branches cross the imaginary axis where  $K_i \approx 1100$  rad/s with parameters as previously

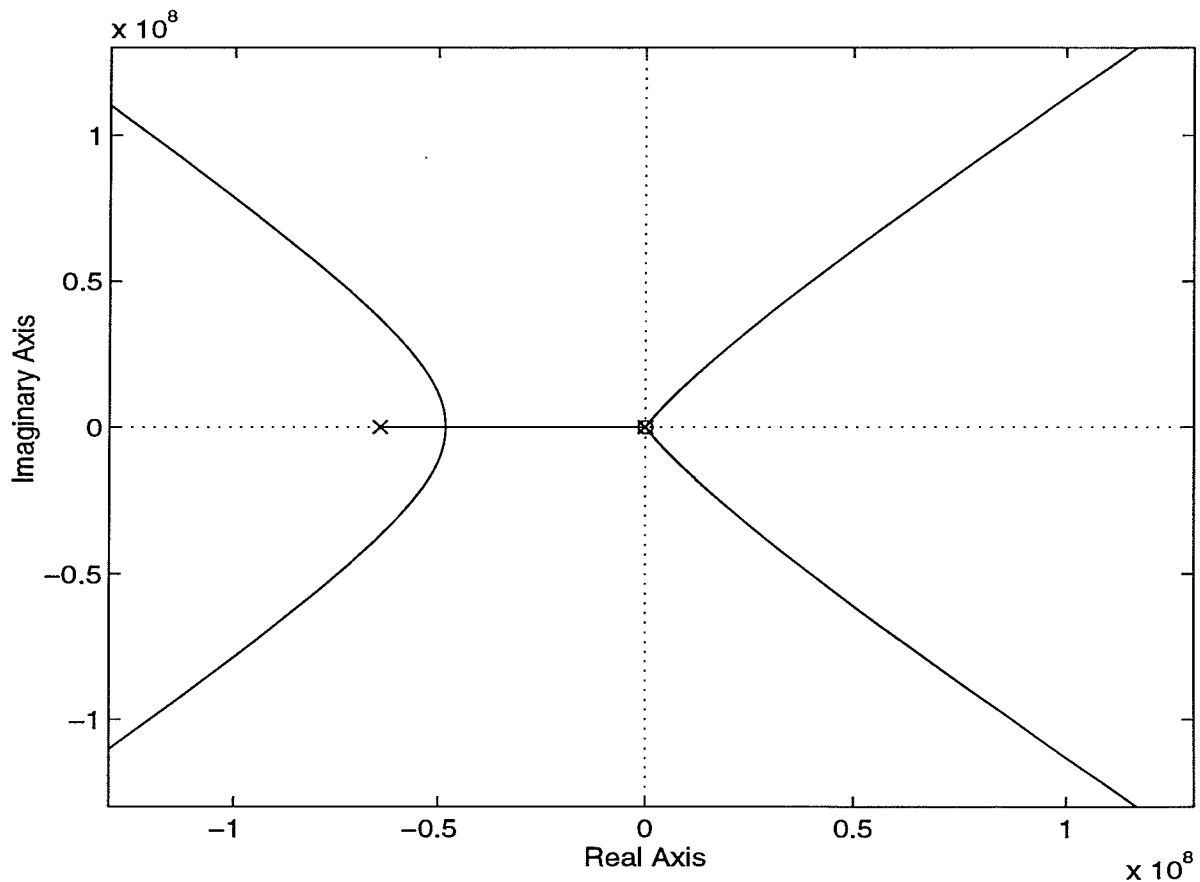


Figure 2.4: Root Locus for Integral Gain

defined. The stability properties vary only slightly with variations in parameters; even if  $L_{II}$  were greatly reduced, the root locus would still have the same properties, as shown by Figure 2.6. Here  $L_{II}$  is arbitrarily set to  $6.18 \mu\text{H}$ , from its previous value of  $618 \mu\text{H}$ . The system goes unstable with  $K_i \approx 73 \text{ krad/s}$ . To be effective, feedback systems should be strictly proportional controllers, with a gain around 130 dB. At 200 kHz switching, the feedback network requires a gain-bandwidth product of 632 GHz, far beyond the capabilities of op amps with the necessary power capabilities.

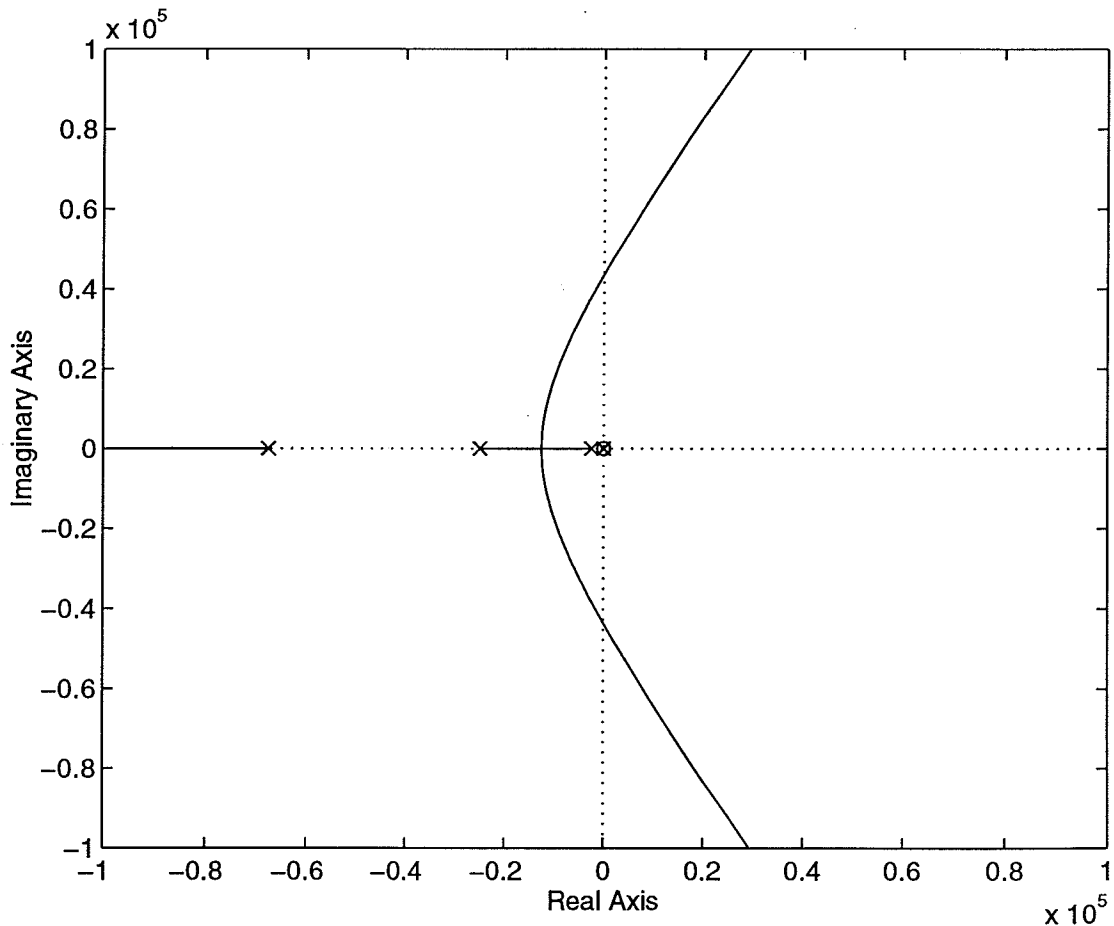


Figure 2.5: Magnified Root Locus of Figure 2.4

Passive filtering can be used instead of feedback or feed-forward compensation, if suitably large capacitors are available. To achieve 9.07 dB of additional ripple attenuation, as is possible with this particular transformer in a feed-forward compensator, output capacitance should be increased by a factor of 2.84, neglecting the effects of ESR. Capacitors cannot be constructed arbitrarily large, and the technologies which exist for relatively large capacitors (hundreds of microfarads) are expensive or result in high

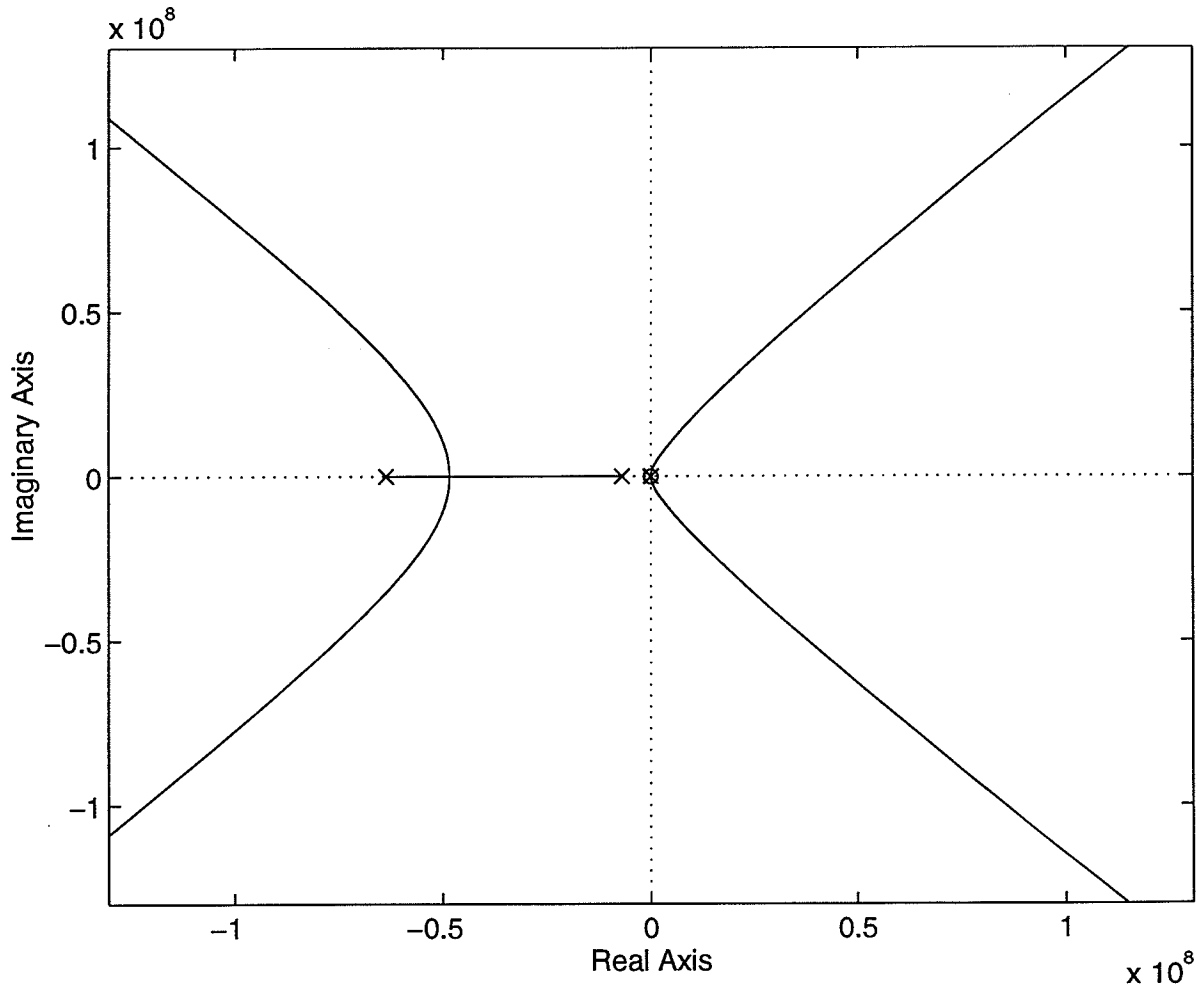


Figure 2.6: Root Locus of Integral Feedback with Reduced  $L_{11}$

ESR. Passive filtering remains the most logical choice if only a small amount of inductor current has to be filtered, but systems with large ripple currents require an active filter. Often a combination is required, as discussed for 60 Hz systems in [9] and [10].

## 2.4 Experimental Results

The time delay effect mentioned in Section 2.2 has been demonstrated in the laboratory. To investigate frequency effects, the circuit shown in Figure 2.7 was used, with the transformer decoupled from an actual power converter. Because the load impedance seen at the secondary when attached to a power converter should be very small, the secondary in the test circuit is shorted.

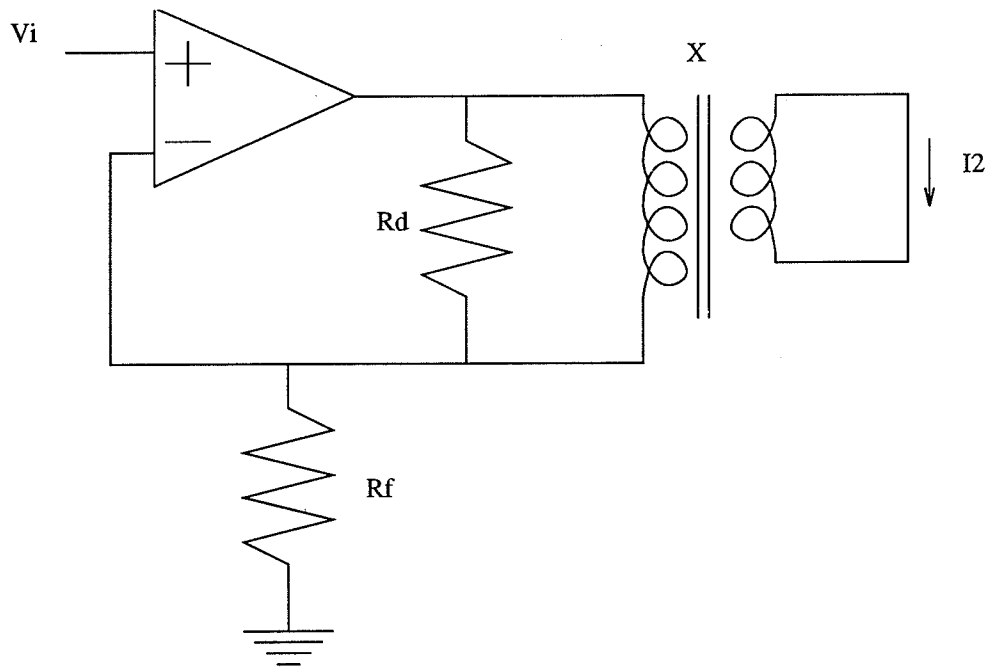


Figure 2.7: Transformer Testing Circuit

Based on values obtained in laboratory experiments, the transfer function of (2.6) and (2.7) gives the Bode plot shown in Figure 2.8. The transformer used, with turns ratio  $a = 100$ , has the following parameters:

$$L_m = 32 \text{ mH}$$

$$L_{ll} = 33.7 \text{ } \mu\text{H}$$

$$C = 16.9 \text{ pF}$$

$$R_l = 9.1 \text{ } \Omega$$

$$R_2 = 3 \text{ m}\Omega$$

$$R_d = 3.5 \text{ k}\Omega$$

$R_d$  is an additional damping resistor experimentally determined through trial and error, used to minimize high-frequency oscillations while not substantially affecting operation.

The effect of the zero at the origin of the  $s$ -plane dominates below 1 kHz. Above this frequency, the effects of the three poles dominate. For typical power converters, the frequencies of interest range from approximately 50 kHz to 2 MHz and above; a Bode plot for the same transfer function as in Figure 2.8 is shown for frequencies from 16 kHz

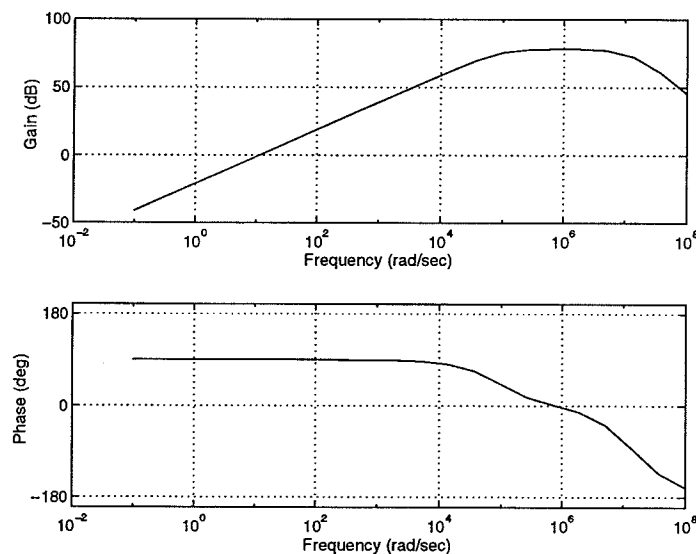


Figure 2.8: Bode Plot for Transformer Model

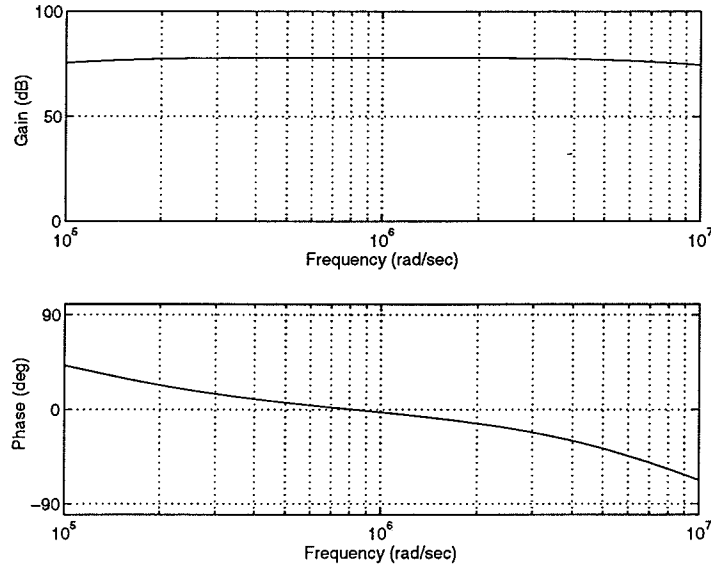


Figure 2.9: Magnified Bode Plot for Transformer Model

(100 krad/s) to 1.6 MHz (10 Mrad/s) in Figure 2.9. In this frequency range, the gain is essentially flat, while the phase delay is nearly linear, corresponding approximately to a time delay.

Experimental results demonstrate the effects of this phase shift. The same transformer for which the Bode plots have been constructed was also placed in a voltage-to-current circuit to measure its frequency response. The data are compiled in Figure 2.10, which also shows the predicted performance from the foregoing analysis.

The time delay imposed by this transformer is considerable in the frequency range of interest, 520 ns at 200 kHz down to 251 ns at 1.0 MHz. Compensation for this effect over a limited frequency range is straightforward: in the voltage-to-current converter shown in Figure 2.7, the load resistor  $R_f$  is augmented by a capacitor  $C_{comp}$  in parallel. The effect is to insert a zero in the transfer function at  $(1/R_f C_{comp})$ . If a zero is added at

1.885 Mrad/s, the time delay drops to 94 ns at 200 kHz and 69 ns at 1 MHz. Results are shown in Figure 2.11, comparing the uncompensated transformer (dashed line) to the compensated transformer (solid line). In addition to reducing the phase lag, compensation also flattens the magnitude response and makes the transfer function closer to ideal.

The resulting feed-forward filter cannot attain perfect performance because of the time delay. Subtracting two triangle waves (the approximate shape of the inductor and compensation currents) separated by some small  $\delta t$  results in a trapezoidal wave, as shown in Figure 2.2, page 14. While the ripple is not eliminated, it is significantly

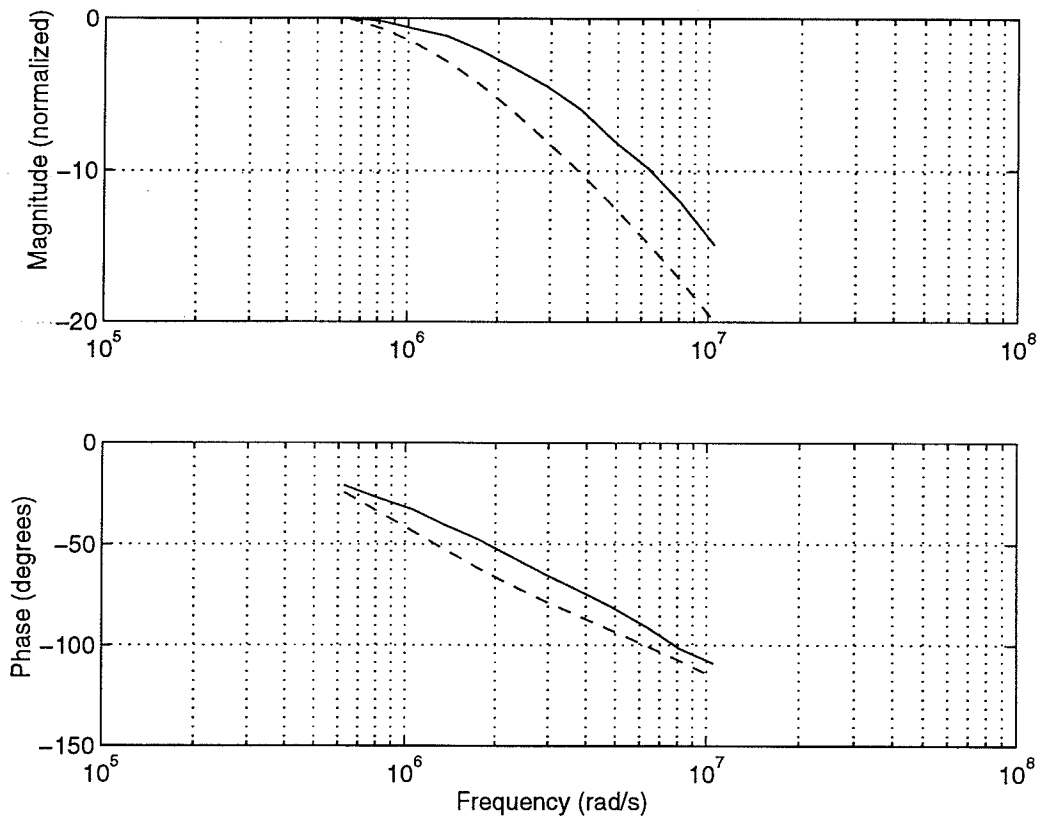


Figure 2.10: Experimental Bode Plot

reduced from the uncompensated power converter. One might consider altering the overall design to eliminate the time delay effect. Some options include introducing zeros to cancel the poles of the current transformer, as in Equation (2.8), or re-designing the current transformer itself. Cancelling the poles is an inherently difficult proposition; it requires accurate knowledge of the response of the transformer, and assumes the relevant parameters are time-invariant. Because most of the relevant terms are parasitics, measurements would have to be made in the final layout and circuit configuration. The more direct route, re-designing the transformer, does offer some hope, but capacitance

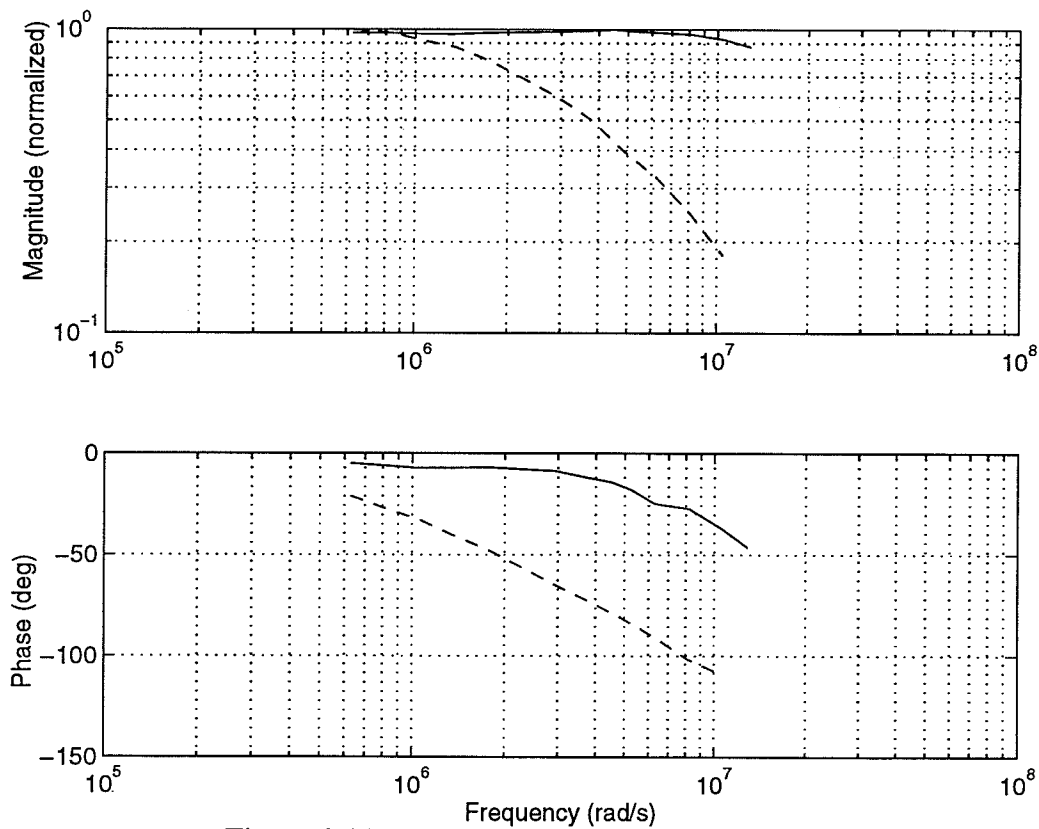


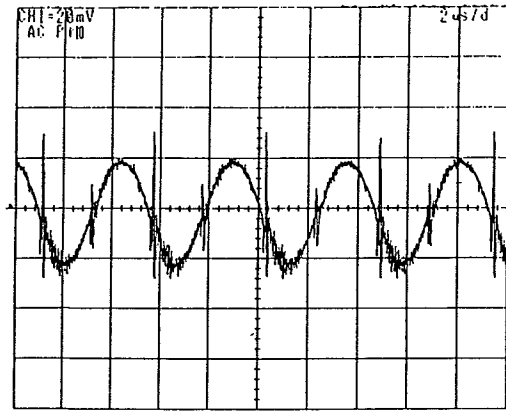
Figure 2.11: Bode Plot: Compensated (solid) and Uncompensated (dashed) Transformer

and leakage inductance will always be a problem. Transformer parasitics limit the ultimate effectiveness of active filters in converters with very high switching frequencies.

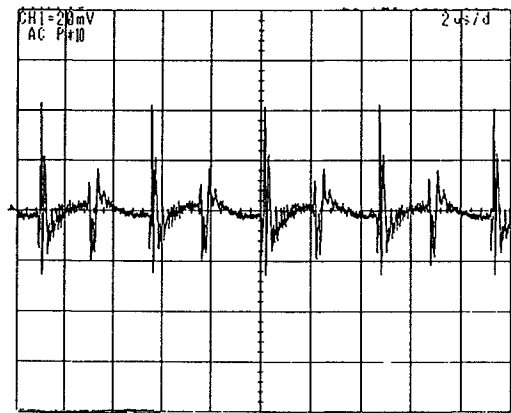
Perhaps a better evaluation would be to compare the feed-forward technique to a feedback method, as described in Section 2.2. Figure 2.12 shows experimental results for a 2 V output at 1 W with no compensation, feed-forward compensation, and feedback compensation. The same op amp is used to generate the correction signal for each (an LF356), and the same current source is used for each (a current transformer driven by an AD847). The feed-forward compensator can be tuned by hand to give substantial attenuation of output ripple. The feedback compensator, however, suffers from noise and instability problems. Even when the feedback compensator becomes stable, the feed-forward compensator is clearly superior. This relates back to the fundamental difference in the two methods: in the feed-forward case, a large voltage, which is independent of any compensation, is sensed and integrated, while in the feedback case, a small voltage, which is made smaller by compensation, is used to generate the compensation current. In both cases, imperfections in the current source limit the amount of compensation possible, but the feed-forward compensator can still achieve some amount of compensation where the feedback compensator cannot.

The noteworthy concept discussed in this section is the fundamental advantage of using feed-forward cancellation rather than feedback cancellation of the output voltage ripple. Experimental results for the designs presented in this section will be shown in Chapter 4 in the discussion of the converter for 1 V at 25 W. In practical

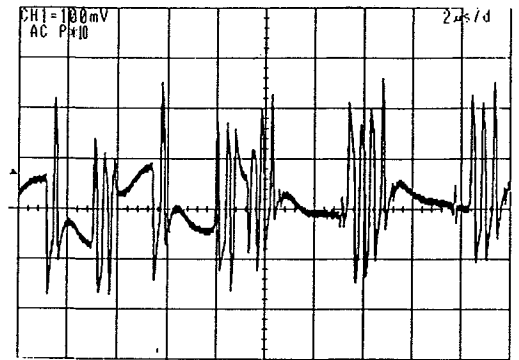
implementation, one would expect feedback to be more sensitive to noise for a variety of reasons, including high gain and small signal magnitudes. Because of the presence of high-frequency switching noise, the feedback compensator becomes unworkable, whereas the feed-forward compensator performs reasonably well.



Uncompensated



Feed-Forward



Feedback

Figure 2.12: Uncompensated, Feed-Forward Compensated, and Feedback Compensated Converter

## CHAPTER 3 ADAPTIVE TIMING CONTROL

Synchronous rectifiers are an important technology for low-voltage power converters. Conventional control techniques for synchronous rectification are very basic, and leave much room for improvement to fully take advantage of the MOSFET used. Most notably, some additional circuitry for adjusting the relative gate signal timing can greatly increase conversion efficiency.

### 3.1 Overview of Synchronous Rectification

Since power MOSFETs became available in the mid-1980's, their use as synchronous rectifiers has been discussed [11]. In fact, there are a few commercially available integrated circuits (ICs) which will control a synchronous buck converter, such as Maxim's MAX767, Linear Technology's LTC1267, and Unitrode's UC3874. The low on-state resistance  $R_{ds(on)}$  of typical MOSFETs motivates the added complexity. The result can be greatly increased efficiency, especially at very low output voltages.

Figures 3.1 and 3.2 show standard and synchronous buck topologies, respectively. In the standard topology, the diode is generally a Schottky rectifier, which has a lower on-state voltage drop  $V_F$  than a p-n junction rectifier. If the designer is willing to pay a little extra in exchange for higher efficiency, a Schottky rectifier rated at higher current than the converter can be used. For comparison purposes, let us consider a buck converter with a rated output of 2 V at 10 A. The designer could choose a 10 A

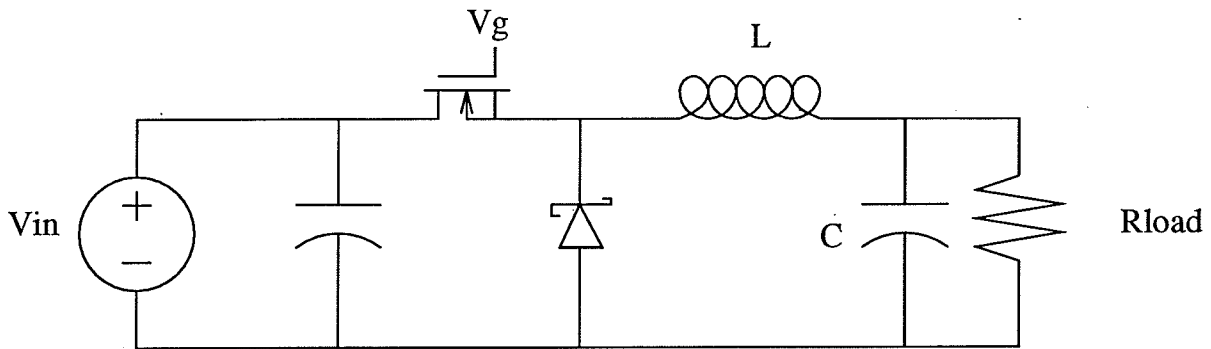


Figure 3.1: Standard Buck Topology

Schottky such as Motorola's MBR1045, with  $V_F = 0.57$  V at 10 A. Alternatively, one could choose a 25 A part such as a 1N5831, with  $V_F = 0.48$  V at 30 A, giving an effective  $V_F \approx 0.40$  V at 10 A. This gives a best-case loss of perhaps 4.0 W while the device is conducting.

A synchronous rectifier implemented with a standard power MOSFET reduces this loss substantially. A 10 A part such as the MTP10N10E gives  $R_{ds(on)} = 0.25$   $\Omega$ . One could choose a 30 A part such as the MTP30N06EL, with  $R_{ds(on)} = 0.05$   $\Omega$ . This gives a best-case loss of  $I^2 R_{ds(on)} = 5.0$  W. While this is, in fact, worse than using a Schottky, MOSFET characteristics improve much more dramatically with increased current ratings and more recent technology; a new 75 A part, the MTP75N03HDL, has an  $R_{ds(on)} = 0.005$   $\Omega$ , resulting in 0.5 W loss. Parts in the 1N5831 family are also physically much larger than parts in the MTP series; a 30 A Schottky in the same package (TO-220), such as the MBR2545CT, has  $V_F = 0.73$  V at 30 A, which implies that the MBR1045 may be the best option where size is a major concern. This analysis

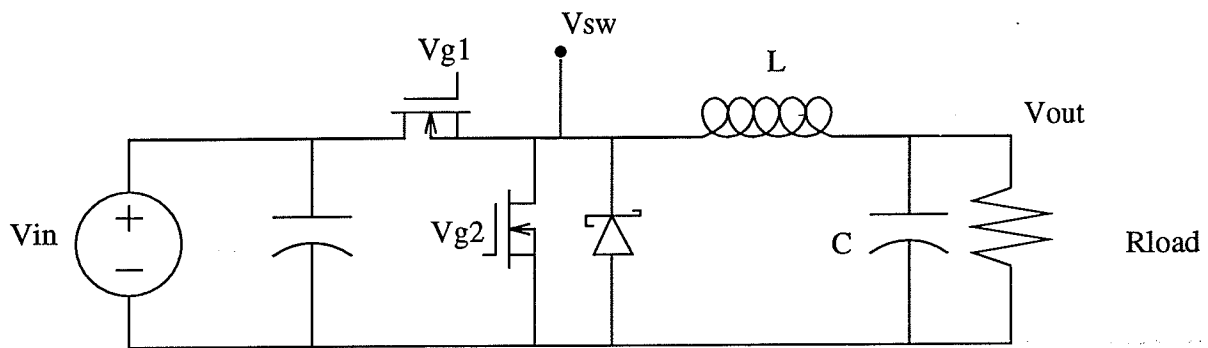


Figure 3.2: Synchronous Buck Topology

fails to consider continuing advancement in technology. Schottky rectifiers are a more mature technology; the greater emphasis in current research is on higher voltage ratings, not lower  $V_F$  ratings. The technology of power MOSFETs continues to advance, with cost as the most significant aspect. Conduction losses can be reduced to negligible levels if the design can tolerate the added expense, while the marginal cost is decreased with each new family of power devices. Synchronous rectification has become common enough that specific MOSFET design techniques are being developed, as discussed in [12].

The remaining consideration is support circuitry. Ideally, exactly one MOSFET should be fully conducting at any given instant. Errors in timing result in shoot-through (both devices conducting) or cause the parasitic diode of the synchronous rectifier to turn on. The need for two controlled switches complicates the analog control circuitry, so attempts have been made to simplify the controller as much as possible. In [13], simple circuits are suggested using combinational logic and comparators to monitor the drain

and source voltages of the synchronous rectifier, which are then used to generate a gate signal. This approach is ultimately limited by the speed of the comparators. In [14], a discrete-time adaptive algorithm is proposed, in which the terminal voltages measured during one cycle are used to generate a gate signal for the next cycle. As with many adaptive algorithms, this approach has a limited region of convergence, which implies poor dynamic performance. Older techniques, described in [11], [15], and [16], use some configuration of transformers with catch windings to directly drive the MOSFET gates. None of these approaches fully solve the basic problem.

Commercial ICs use a much simpler approach. Every power MOSFET has a parasitic body diode anti-parallel to the basic MOSFET. Commercial ICs take advantage of this to simplify the timing issue: By inserting some dead time between the two gate signals, during which both gates are held low, one can avoid having both MOSFETs conducting simultaneously. During this dead time, the body diode of the synchronous rectifier carries the inductor current. This scheme has several drawbacks. The body diode is typically not a high quality diode, with reverse-recovery losses large compared to fast power rectifiers. The common practice to avoid loss in the body diode is to add a Schottky rectifier anti-parallel with the MOSFET. The resulting circuit adds cost and does not make full use of the MOSFET—the Schottky rectifier has not been replaced, merely augmented. Finally, although the actual length of the dead-time is not critical to operation, it does limit the efficiency, particularly in the absence of an additional Schottky rectifier. The effects of various timing methods on efficiency is discussed in

depth in [17]. While effective, the approach used in commercial ICs leaves room for improvement.

### 3.2 Theoretical Development of Correlation Technique

Ultimately, the goal of replacing the rectifier in a buck converter with a MOSFET synchronous rectifier is to reduce input power for a given output power, which increases the overall efficiency. Given fixed input and output voltages, the only degree of freedom remaining is the relative timing of the gate signals. Intuitively, one might expect the efficiency to depend on the timing, with a single best point where the MOSFETs commute optimally. Experiment verifies the existence of a single optimum, which depends on temperature, load current, gate resistance and capacitance, and other unknown factors. The power loss is a non-monotonic function of switch timing with a single minimum. A correlation-based control scheme can be used to maximize efficiency or minimize input power.

First, let us consider a general approach to correlation-based control. For continuous functions, this technique has been developed in depth in [18], while a similar discrete-time method is discussed in [7]. Here, the technique is extended to switching functions. The goal of the control technique is to maximize or minimize a given cost function  $J$ . The present discussion is restricted to minimization, but the only difference is a sign change. Suppose there is some switching function  $x$  which affects  $J$ . Define  $x$  as follows:

$$\begin{aligned} tri(t) &= 2 \left| 1 - \frac{2 \text{mod}(t, T)}{T} \right| - 1 \\ x(t) &= \text{sgn}(\delta - tri(t)) \end{aligned} \quad (3.1)$$

making  $tri(t)$  a triangle wave and  $x(t)$  an asymmetrical square wave with duty ratio  $\delta$ . In a pulse-width modulation (PWM) system, the most appropriate control variable is  $\delta$ , because  $tri(t)$  is relatively easy to generate and a comparator can generate  $x(t)$  from  $tri(t)$  and  $\delta$ . The implicit assumption is that  $\delta$  is always positive, but an equivalent definition can be made such that  $\delta < 0 \Rightarrow x < 0$ . In either case,  $\delta$  must be constrained to be non-zero.

Armed with these definitions, a nonlinear control law can be formulated as follows:

$$\delta(t) = -k \int_0^t x J dt = -k \int_0^t x \frac{\partial J}{\partial \delta} \dot{\delta} dt \quad (3.2)$$

The actual implementation is of the first equality, while the second equality lends itself to further analysis. The gain  $k$  is somewhat arbitrary but affects noise immunity and response time. Taking the derivative of both sides and combining terms gives

$$\dot{\delta} \left( 1 + kx \frac{\partial J}{\partial \delta} \right) = 0 \quad (3.3)$$

Examination of either (3.2) or (3.3) can show that when  $(\partial J / \partial \delta)$  is zero, implying  $J$  is

minimized with respect to  $\delta$ , then  $\delta$  is no longer changing. Because  $\delta$  is constrained to be non-zero, there is no trivial solution. Further examination shows that when  $(\partial J/\partial \delta)$  is negative,  $\delta$  is increasing, while when  $(\partial J/\partial \delta)$  is positive,  $\delta$  is decreasing, consistent with approaching the minimum of  $J(\delta)$ . Simulation results for a hypothetical cost function  $J = (\delta - 1)^2$  are shown in Figure 3.3, including noise in  $J$ . The simulations verify the foregoing discussion rather well—essentially perfect steady-state behavior, with response time and noise immunity determined by the gain  $k$ .

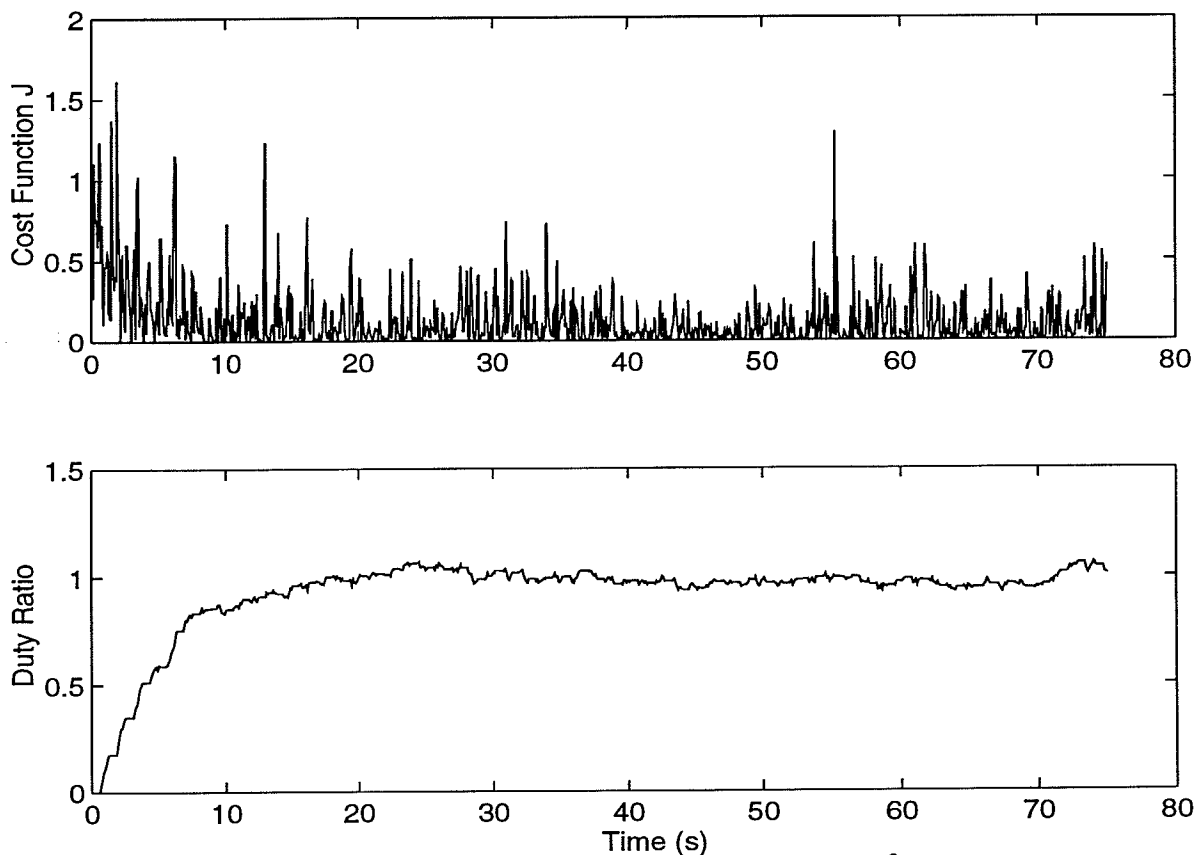


Figure 3.3: Simulation Results for  $J = (\delta - 1)^2$

### 3.3 Development of Timing Control

Now consider applying the technique described in Section 3.2 to the problem of gate signal timing for a synchronous rectifier. During the two transition times of each cycle, the inductor current  $i_L$  must commute from one device to the other. This process is affected by many factors, including gate capacitance and stray inductance. To justify using a synchronous rectifier along with relatively complicated control circuitry, choose the cost function  $J$  to be the input current  $I_{in}$  in order to optimize efficiency.

Alternatively, the choice could be  $J = P_{in} = V_{in} I_{in}$ , more accurately reflecting the actual desired goal.  $V_{in}$  is not subject to control, however, and an input capacitor should keep it essentially constant even during transients. Experiments have shown that the algorithm performs well without the additional information provided by  $V_{in}$ .

A quasi-static analysis gives a qualitative form for  $J(\delta)$  by considering only conduction losses. Assume for simplicity that turn-on is immediate, while turn-off takes some amount of time. The main current being commutated is the inductor current  $i_L$ .

When a MOSFET is on, the conduction loss can be approximated as a resistive drop  $R$ .

If the diode turns on, there is some constant-voltage drop, as well as some resistive drop.

For convenience, approximate the effective resistance of the diode to be the same as the

on-resistance of a MOSFET. Let  $\delta'$  represent the time difference for actual conduction in the two MOSFETs. Then some circuit analysis shows:

$$P_{lost} = i_L^2 R + \frac{\delta'}{T} \left( V_d i_L u(\delta') + \frac{V_{in}^2}{R} u(-\delta') \right) \quad (3.4)$$

for a total conduction interval  $T$ , where  $u(\bullet)$  is a unit step function. In actual operation, parasitic inductance, resistance, and capacitance combine to insert some time delay  $\delta_o$  between commanded turn-off and actual turn-off. Equation (3.4) holds for measured signals if  $\delta'$  is replaced by  $(\delta - \delta_o)$ . For typical values of  $R$ ,  $V_d$ ,  $i_L$ ,  $T$ , and  $\delta_o$ , Figure 3.4 shows  $P_{lost}$  as a function of  $\delta$ .

Following the development in Section 3.2, the algorithm requires a square-wave type of variable. Experiments show that the algorithm works effectively using a

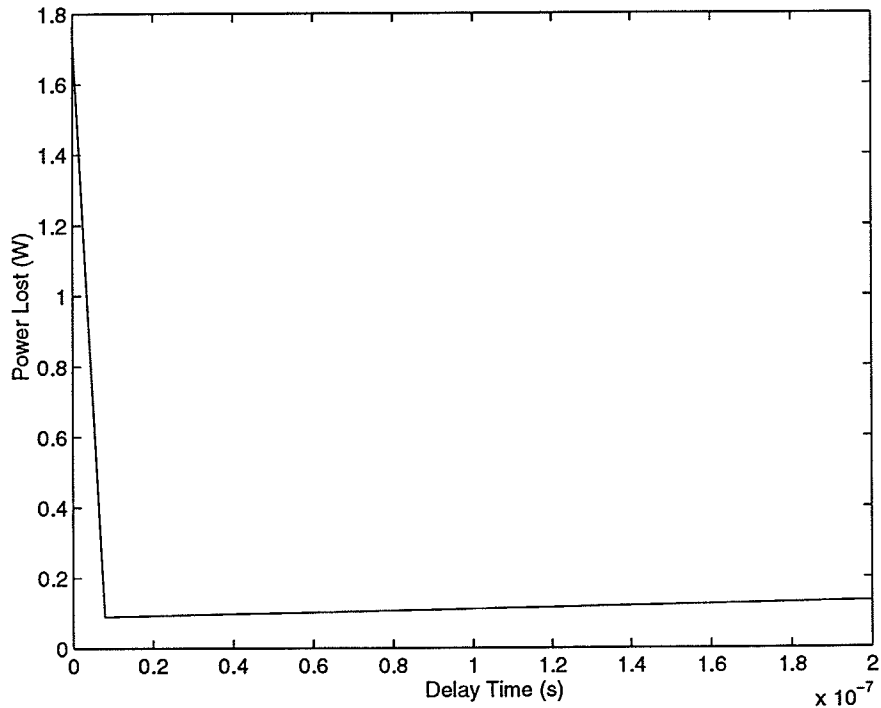


Figure 3.4: Theoretical Loss as  $\delta$  Varies

switching function instead: rather than oscillating between +1 and -1,  $x$  oscillates between +1 and 0. For power conversion, the gate signals  $V_{gs1}$  and  $V_{gs2}$  have to be generated as switching functions displaced by some  $\delta$ . Some combination of the two gate signals could be used to create  $x(t)$ . In the original implementation for a 5 V input to 2 V output at 1 W, the high-side MOSFET is a P-channel device, which is “active low,” i.e., the device conducts when  $V_{gs1} = (V_{g1} - 5)$  is negative. A switching function with duty ratio  $\delta$  can be generated by simply using the difference in gate voltage,  $\Delta V_g = (V_{g2} - V_{g1})$ , which can be easily measured with a single op amp.

The algorithm requires information about the input current. The standard method for current measurement involves a current shunt, a small resistor placed in series with the rest of the converter. Any resistance conducting the full load current introduces another loss term; while this loss could be considered minimal compared to the increase in information for control, any source of loss should be eliminated if possible. An alternative method involves an input inductor. Inductance at the input is useful for reducing current ripple at the source, if appropriate capacitance is included. Many energy sources, particularly batteries, respond poorly to current ripple. Adding an input inductor provides a method for direct measurement of the time derivative of input current. As compared to a current shunt, an input inductor provides both useful information for control and useful functionality for improving input characteristics, while adding minimal loss.

Combining this discussion with the results of Section 3.2, the final algorithm used in a converter with one P-channel device is

$$\delta(t) = -k \int_0^t (V_{g2} - V_{g1}) V_{L_{in}} dt \quad (3.5)$$

Implementation issues and results are discussed in the following section. The algorithm of Equation (3.5) conforms to the general structure discussed in Section 3.2, and therefore should give consistent results regardless of device parameters or other factors which would affect  $J(\delta)$ . The only issue left unresolved is that of local minima. If such minima exist, appropriate limits on  $\delta$  are required to eliminate any problems.

### 3.4 Implementation and Results

The technique described above has been investigated in detail using the 2 V, 1 W converter mentioned in Section 2.4. A full schematic can be seen in the Appendix. The most obvious differences between the actual converter and the description given in Section 3.3 are the actuation method and the gate voltage measurements. In order to make use of commercially available parts, the PWM system had to be somewhat modified. Essentially,  $tri(t)$  as defined in (3.1) has been shifted to have no dc component; a separate voltage mode and sensorless current mode loop sets the basic duty ratio  $D$ , and the adaptive loop sets the duty ratio of  $Q_1$  to be  $D + \delta$ . So long as the final gate signals end up the same, shifting the PWM process has no net effect on operation.