

Sigma-Delta Modulation of Multi-Phase High Frequency Converters

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Abstract— A power conversion control architecture is proposed that merges advanced digital modulation techniques, high frequency resonant converters, and multi-phase converters. If a converter's switching frequency is high enough, the converter may be turned on and off quickly to modulate power flow. The proposed system is composed of several high frequency converters connected in parallel, only a few of which are active at a given time to regulate the output voltage. The number of active converters is determined through a sigma-delta modulation process. The specific converter enable signals are generated by a balancing algorithm that ensures approximately equal effective duty ratio and switching frequency for all phases. An output voltage regulator, here implemented as a PI loop, completes the system. The method has been simulated for an eight-phase closed-loop system. Experimental results are shown for a four-phase open-loop system with an external command that corresponds to the effective duty ratio of the power converters.

I. INTRODUCTION

Trends in the power converter industry include a push to higher switching frequencies for reduced size, a migration to digital control techniques, and the use of multi-phase converters. In the present work, these trends converge in a new control scheme for a multi-phase high frequency power converter. Specifically, sigma-delta modulation is used to switch converters on and off at a high rate to regulate output voltage.

If the switching frequency of a power converter is high enough, e.g. 10 MHz, the converter may be switched on and off just as fast as a conventional converter switches. This approach was first proposed in [1] for class E converters, and has also been applied to class Φ_2 converters [2, 3]. In all previous studies, voltage hysteresis control was used to enable and disable converters. In [1], a Vernier scale with hysteresis was proposed for a multi-phase converter. Hysteresis control is a type of asynchronous delta modulation [4].

Hysteresis control is relatively easy to implement in an analog controller, but far more difficult to achieve in a digital controller. Hysteresis is an inherently asynchronous process, whereas digital controllers that act on analog signals must use

synchronous processes. Digital controllers are preferable, though, for many reasons, ranging from user interface to precision to field upgradeability. Digital controllers are also able to implement advanced, nonlinear control methods that are impractical in an analog circuit. The synchronous nature of digital processes corresponds to sampled-data techniques.

A conventional digital controller for a power converter samples voltages (and possibly currents) at a fixed rate and uses that information in a discrete-time feedback controller. Instead of direct action on the voltages (as in hysteresis and other geometric techniques), linear or nonlinear feedback controllers in the z domain are used to create a duty cycle command. The duty cycle is the input to a uniformly sampled pulsewidth modulation (PWM) process. A typical uniform PWM process with n bits of resolution is constructed with an n -bit counter that increments at 2^n times the output frequency and a comparator.

Sigma-delta (Σ - Δ) modulation, a type of synchronous delta modulation [4], was used in [5] to enhance the precision of a digital PWM process. In a digital controller with high switching frequencies, the clock rate for the counter can become unmanageable. For example, a 1 MHz PWM signal with 8 bits of resolution would require a base clock frequency of 256 MHz—achievable, but highly undesirable. Twelve bits of resolution would require a base clock frequency of 4 GHz, which is achievable only at a prohibitively high cost. Now suppose that the duty cycle command is encoded with m bits of resolution, but the PWM process is only capable of n bits of resolution (where $m > n$). For example, a 4-bit PWM process with a 16 MHz clock could be used to generate 1 MHz switching signals, even though the desired PWM resolution is 12 bits. With Σ - Δ modulation, the extra resolution in the input ($m-n$ bits) is an error term that is driven to zero over time by varying the duty ratio of the basic PWM process, so a low value for n and a low clock frequency may be used. A first-order Σ - Δ modulator is shown in Fig. 1. The feedback on the error ensures that the process has sufficient resolution over a

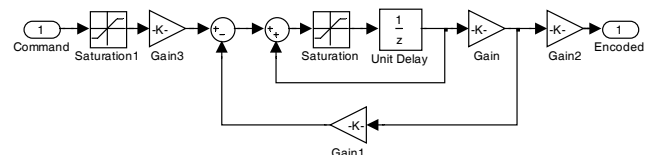


Fig. 1. First-order Σ - Δ modulation process. Gains implement left and right shifts.

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long time period.

The present work combines the basic principles of Σ - Δ modulation, as applied in [5] to power converters, with high-frequency power converters that are alternately enabled and disabled. The combination has the potential for high efficiency and small size, due to the high frequency resonant power converter, with all of the positive attributes of digital control, such as user interface, reconfigurability, and the potential for sophisticated nonlinear controllers. A similar concept was applied to a single-phase class D resonant converter in [6]. The present work extends this concept substantially to address multi-phase power converters. Section II describes the new modulation process. Section III shows simulation results of the modulator combined with Φ_2 power converters. Section IV shows experimental results of the combined system. Important VHDL code is included in an appendix.

II. PROPOSED MODULATION PROCESS

A multi-phase VHF power converter is not directly amenable to PWM, so a new modulation process has been developed for the different requirements. The assumption in [5] is that the actuator is a conventional hard-switched converter, such as a buck converter, whose duty ratio must be controlled. For highly resonant topologies, such as class E and class Φ_2 converters, duty ratio variation should be avoided. Rather, the converter should be turned on and off as

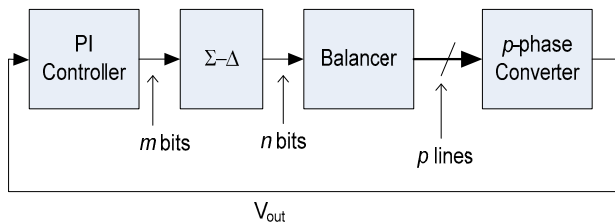


Fig. 2. Proposed control and modulation process.

Command	Time		
	t_0	t_1	t_2
1	0	p	p-1
1	1	0	p
...
1	y	y-1	y-2
0	y+1	y	y-1
...
0	p-1	p-2	p-3
0	p	p-1	p-2

Fig. 3. Balancing method, indicating which phases are enabled as time progresses for a commanded value y .

in [1]. If several converters are connected in parallel, a fraction of the converters may be active at any time. If there are p converters total and q are active, the effective duty ratio of the converter system is q/p . This effective duty ratio can be determined through a Σ - Δ process.

Fig. 2 shows the proposed modulation process. A conventional first-order Σ - Δ process has been used. Higher-order Σ - Δ processes may be used instead with minimal changes. The output of the Σ - Δ process, y , is encoded in n bits. The power converter system contains $p = 2^n$ identical converter phases.

The block in Fig. 2 labeled “Balancer” converts the integer-valued command y into p enable (binary) signals. If a simple thermometer code were used here, some phases would be enabled almost all of the time, some would rarely be enabled, and some would switch frequently. Instead, the phases are treated as equals in a ring with a beginning point that shifts over time. The process is shown schematically in Fig. 3. Corresponding VHDL code, synthesizable with Quartus II for an Altera EP2C50F484I8 FPGA, is given in the appendix for the case $p = 4$.

Fig. 4 shows computed switching frequency for a simulated system similar to that shown in Fig. 2, operating open-loop with a sinusoidally varying effective duty ratio. In this case, $m = 12$, $n = 3$, and $p = 2^3 = 8$. The beginning point in the ring shifts at a frequency that is a multiple of the sampling frequency, which is fixed at 1 MHz. As this multiplier increases, the effective switching frequency of each phase decreases monotonically. The effective switching frequency varies less than 2% among the phases, as indicated by the standard deviation. All eight phases have the same long-term average duty ratio.

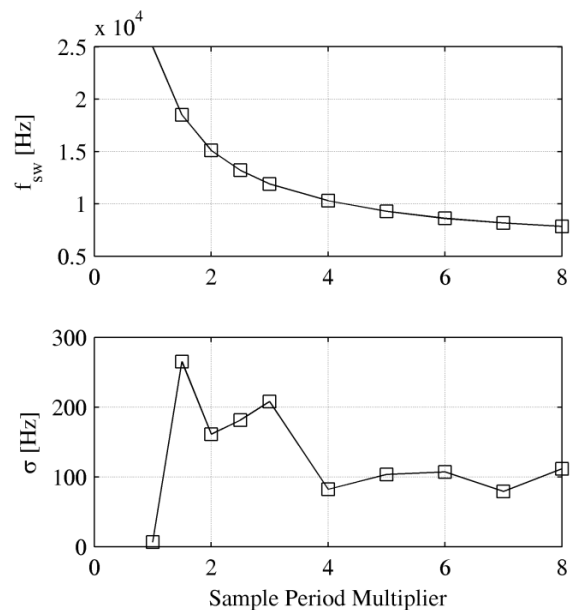


Fig. 4. Effective switching frequency f_{sw} and its standard deviation σ for an 8-phase balanced Σ - Δ process with a sampling frequency of 100 kHz.

III. INTEGRATION WITH HIGH FREQUENCY CONVERTERS

The output of the Σ - Δ modulator described above is a set of enable signals for high frequency converter phases that are connected in parallel. For the present study, class Φ_2 boost converters were used; other converter types with fast start-up dynamics may be used as well. A class Φ_2 converter can be approximated as a current source with a magnitude that depends on switching frequency, component values, and terminal voltages. Fig. 5 shows simulation results for a system with eight class Φ_2 converters, a proportional-integral (PI) regulator for the output voltage, a Σ - Δ modulator to convert the 12-bit PI output into a 3-bit command, and a balancer to convert the 3-bit command into eight balanced enable commands. The straight-line ripple results from a varying number of active phases, and the small-signal ripple (visible only as a thick line in this zoomed-out view) results from the high-frequency switching of the individual phases. The dip at the beginning is a start-up transient in the PI loop. This method incorporates conventional digital control (a PI loop), advanced modulation techniques (Σ - Δ), and high frequency power conversion (class Φ_2 converters) in a multi-phase system. More sophisticated voltage regulation methods, such as energy-based methods [7], may be easily incorporated.

IV. EXPERIMENTAL RESULTS

An experimental system was used to validate the simulation results discussed above. First, the digital circuit was validated. The system was composed of an analog command on a 3.3 V scale, a 12-bit analog-to-digital converter (Analog Devices AD7276), a 2-bit first-order Σ - Δ process, and a four-output balancer. The system was clocked at 1.85 MHz, using a 24 MHz clock source and a divide-by-13 block. The logic was implemented in an Altera EP2C50F484I8N FPGA on a Microtronix Firefly II module.

Fig. 6 shows a typical set of waveforms. Here, the analog input is 1.49 V. The mean duty ratio of the four enable signals is 0.4266. The system oscillates between enabling one converter and enabling two converters. Which one or two converters are enabled, though, shifts over time. Therefore, all

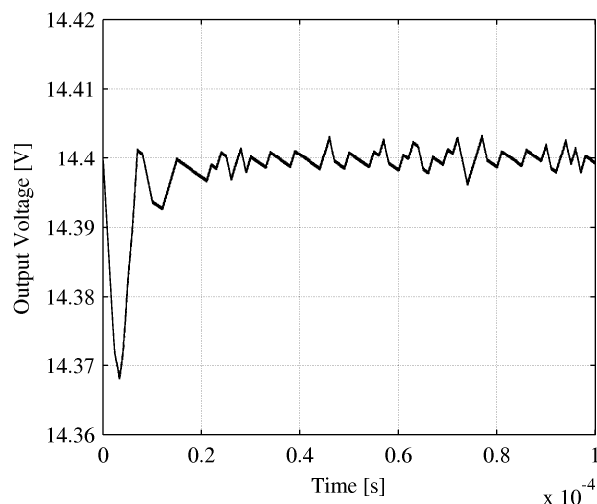


Fig. 5. Simulated output voltage for eight-phase converter with Σ - Δ modulation.

four enable signals have duty ratios near the mean, with a total standard deviation of 0.0027. Although the update rate is 1.85 MHz, the effective switching frequency of the enable signals is approximately 154 kHz. The balancer is updated every other sample of the Σ - Δ loop.

Fig. 7 shows the variation in duty ratio as the input command varies. As expected, the effective duty ratio D_{eff} is linear with the command x , such that

$$D_{eff} = 0.302x - 0.0233 \quad (1)$$

The gain, 0.302, comes from the fact that the full-scale input is 3.3 V. The offset is thought to result from voltage drop in the connections.

Next, this controller was applied to a four-phase power converter. Each phase was a class Φ_2 converter, built according to the schematic in Fig. 8. Parameters are shown in Table 1. Each converter switches at 10.18 MHz and has an “enable” input. Fig. 9 shows gate and drain voltages for the main MOSFET (Q1) and the rectifier input voltage (i.e. voltage on C1). There are multiple resonances in the system to achieve proper voltage waveshapes [2]. One of the challenges in building a multi-phase converter with this

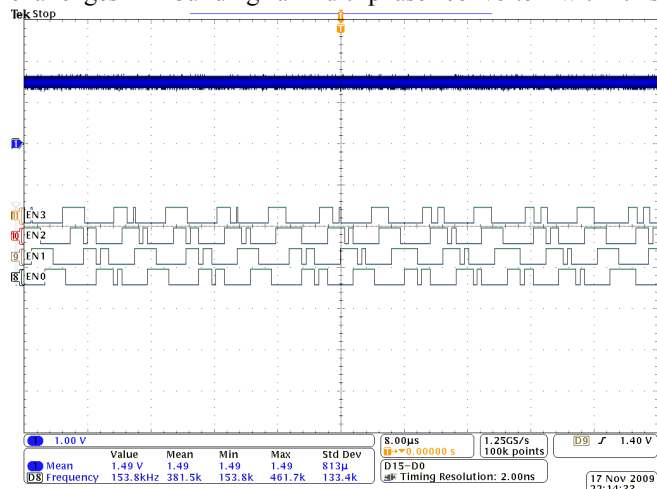


Fig. 6. Sample waveforms of sigma-delta modulator with balancer. From top: analog command, enable signals for phases 3, 2, 1, and 0.

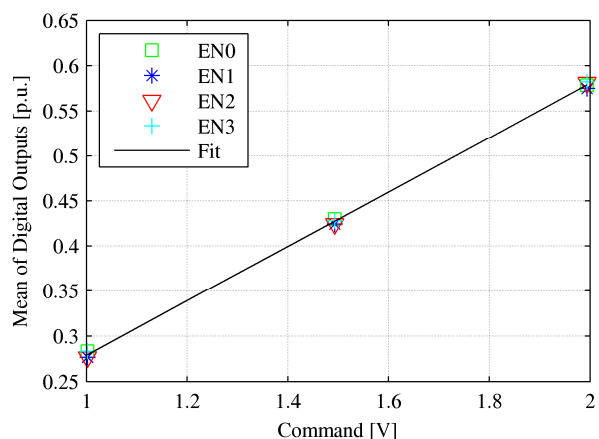


Fig. 7. Relationship between the analog command and the duty ratios of the enable signals (digital outputs).

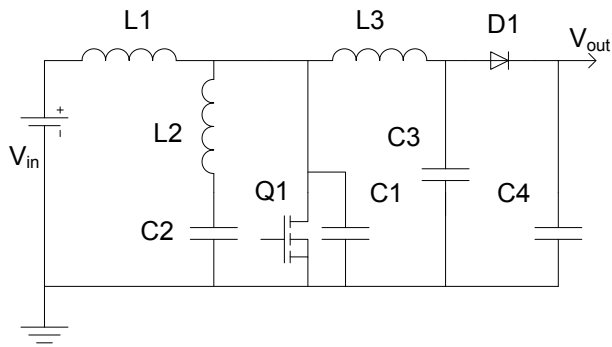


Fig. 8. Schematic of a single Φ_2 boost converter.

TABLE 1. PARAMETERS FOR Φ_2 BOOST CONVERTERS.

Input Inductor L1	35.5 nH
Resonant Inductor L2	18.5 nH
Output Inductor L3	35.5 nH
MOSFET Extra Capacitor C1	6.8 nF
Resonant Capacitor C2	3.3 nF
Output Resonant Capacitor C3	1.5 nF
Output DC Capacitor C4	5 μ F
Main MOSFET Q1	Si7726DN
Output Rectifier D1	MBRA340T3

topology is tuning all of the tanks. The boards used in the final test were all built with components whose nominal values are given in Table 1. A compromise switching frequency and a compromise duty cycle were selected to give the most uniform performance.

Results from the four-phase testing are shown in Fig. 10. In this test, the output was connected to an electronic load configured as a constant voltage (9.5 V). As the input command varied, the output current varied. The relationship is expected to be linear, but is nonlinear in the experimental system. A quadratic curve fit is indicated on Fig. 10. Possible explanations include the variation between the phases and an observed delay of approximately 80 ns between the enable signals and the gate waveforms. That is, the gate driver did not start switching until approximately 80 ns after being enabled. This time delay is manageable but not negligible on this time scale, so it may partially explain the nonlinearity in the system response.

V. CONCLUSIONS

A new control method for multi-phase high-frequency converters was derived and demonstrated. The method combines conventional digital control, Σ - Δ modulation, and VHF conversion techniques. Simulations indicate that the converter phases can be modeled as current sources and the output voltage varies linearly with commanded duty ratio. Experimental results show a nonlinear but monotonic input-to-output characteristic. Future work will improve the individual phases and the start-up characteristics to improve linearity.

VI. ACKNOWLEDGMENTS

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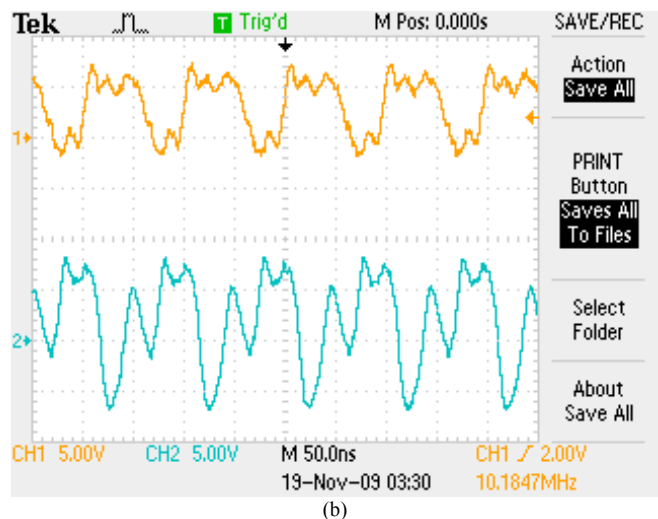
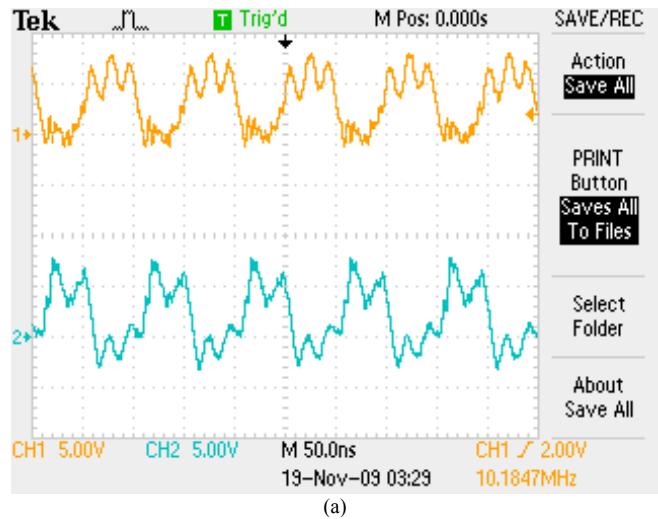


Fig. 9. Key waveforms in Φ_2 converter. (a) Gate-source (channel 1, top) and drain-source (channel 2) voltages of Q1. (b) Gate-source (channel 1, top) voltage of Q1 and rectifier input voltage (channel 2, voltage on C3).

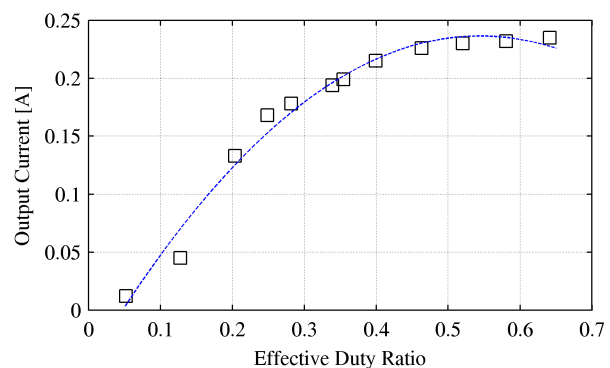


Fig. 10. Output current of the four-phase system as a function of effective duty ratio (given by (1)).

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APPENDIX: VHDL CODE FOR BALANCER

```

LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_unsigned.all;

ENTITY balancer_2by4 IS
    PORT
    (
        clk      : IN STD_LOGIC;
        reset    : IN STD_LOGIC;
        valin    : IN STD_LOGIC_VECTOR(1 DOWNTO 0);    -- 2-bit value to encode
        divider  : IN STD_LOGIC_VECTOR(3 DOWNTO 0);    -- clock divider for rotation
        valout   : OUT STD_LOGIC_VECTOR(3 DOWNTO 0)    -- 4-bit pseudo-thermometer code
    );
END balancer_2by4;

ARCHITECTURE behavioral OF balancer_2by4 IS
    SIGNAL counter : STD_LOGIC_VECTOR(3 DOWNTO 0);
    SIGNAL rotation : STD_LOGIC_VECTOR(1 DOWNTO 0);
    SIGNAL y       : STD_LOGIC_VECTOR(3 DOWNTO 0);
    SIGNAL rot0, rot1, rot2, rot3 : STD_LOGIC_VECTOR(3 DOWNTO 0);
BEGIN
    rot0 <= "00" & rotation;
    rot1 <= ("00" & rotation) + 1;
    rot2 <= ("00" & rotation) + 2;
    rot3 <= ("00" & rotation) + 3;

    y(0) <= '1' when (rot0(1 DOWNTO 0) < valin) else '0';
    y(1) <= '1' when (rot1(1 DOWNTO 0) < valin) else '0';
    y(2) <= '1' when (rot2(1 DOWNTO 0) < valin) else '0';
    y(3) <= '1' when (rot3(1 DOWNTO 0) < valin) else '0';

    valout <= y;

PROCESS (clk, reset) IS
BEGIN
    if (reset = '0') then
        counter <= "0000";
        rotation <= "00";
    elsif (rising_edge(clk)) then
        counter <= counter + 1;
        if (counter = divider) then
            rotation <= rotation + 1;
            counter <= "0000";
        end if;
    end if;
END PROCESS;

END behavioral;

```