A Comparative Efficiency Study of Silicon-based Solid State Transformers

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Abstract—Solid state transformers (SSTs) have lower physical profiles than traditional 60 Hz transformers and provide active control of power flow. However, they are not as efficient as traditional 60 Hz transformers because of the presence of power electronic converters. This work presents an analytical loss calculation model of an SST. It evaluates conduction loss, switching loss and transformer loss in four candidate SST topologies. Loss breakdown under both rated-load and light-load conditions are compared for all four configurations.

Index Terms—Solid State Transformer, Efficiency, Soft Switching

I. INTRODUCTION

Power electronic converter-based solid state transformers (SSTs) have become attractive during recent years. Thanks to high-frequency modulation, the volume and weight of SSTs can be much smaller than those of conventional 60 Hz transformers [1]. More importantly, SSTs provide active power flow control and ports for distributed generation (DG) sources at the distribution level; such ports are essential to the future renewable energy power grid [2]. However, an SST must have a power efficiency profile similar to that of a conventional passive transformer (typically 97%).

In an SST, the presence of power converters reduces efficiency by introducing conduction and switching losses. Soft switching is one feasible solution, facilitated either by adding auxiliary devices (auxiliary resonant commutated pole, or ARCP) [3] or by using leakage inductance of high-frequency transformers (dual active bridge converter, or DAB) [4] [5]. However, soft switching adds circulated energy, trading conduction loss for switching loss.

Fig. 1 shows four potential 20 kVA 7.2 kV/240 V SST configurations using silicon-based power device. All have power electronic converters that can actively control power flow; therefore, they are categorized as SSTs. These topologies are: (1) a back-to-back voltage source converter (VSC) with a conventional 60 Hz transformer (SST1); (2) a three-stage SST with a two-level input-series front end (SST2); (3) a three-stage SST with four-level flying capacitor front end; and (4) a single-stage ac-ac DAB converter-based SST (SST4).

This paper first reviews the operational principles for all four SST topologies and zero voltage switching (ZVS) commutations using ARCP or leakage inductance. It then presents analytical loss calculations of both semiconductor device and transformer and illustrates the loss breakdown in the SST. Finally, it comparies the efficiency of all four topologies under different load conditions and identifies key targets for loss reduction.

II. OPERATION PRINCIPLE

A. SST Configurations

The following briefly reviews the hardware configuration and operational principles of four SST topologies:

1) Back-to-back VSC with 60 Hz transformer (SST1): SST1 is a cascade connection of a 60 Hz passive transformer and a low-voltage ac-dc-ac converter. It lacks the advantage of a high frequency transformer; however, it does have power flow controllability. So it is defined as an SST configuration. It sets a base line for evaluation of the efficiency of SSTs.

2) Three-stage SST with two-level rectifier (SST2): SST2 uses input-series-output-parallel configuration because available silicon-based devices are unable to block peak voltage on the 7.2 kV side. Each two-level rectifier converts one-third of the input voltage to a 4 kV dc bus. Three dc-dc DAB converters, whose outputs are parallel-connected, provide galvanically isolated power conversion to a 400 V dc bus. An inverter converts low voltage dc to utility ac voltage. SST2 is the most complex configuration. However, It has the full features of an SST: compact high frequency transformer, power flow control, power factor correction, and a low voltage dc bus for DG connection.

3) Three-stage SST with multi-level rectifier (SST3): SST3 is similar to SST2 at the DAB and inverter stages. The difference is at the rectifier stage. SST3 uses one flying capacitor multilevel ac-dc converter to provide a 12 kV dc bus for three parallel-connected dc-dc DAB converters.

4) Single stage ac-ac DAB converter (SST4): SST4 uses an direct ac-ac version of a DAB converter [5]. It comprises three ac-ac DAB converters in an input-series-output-parallel connection. This simple topology controls only active power and lacks a dc port for renewable energy.

B. Soft Switching Process

1) ARCP: ARCP adds a bi-directional switch pole between the neutral point of dc bus and the midpoint of a main switch leg. Auxiliary switches are turned on during the main switching transient and they provide enough inductive energy...
to resonate with snubber capacitors. This limits the dv/dt of the main switches during transients and achieves ZVS for both the main switches and auxiliary switches. There is fixed and variable timing for ARCP [6]. For simplicity, only fixed-timing is analyzed here. ARCP is always used for switching transients from a diode to a transistor (Fig 2(a)). For transistor to diode switching, the auxiliary switches are not used at heavy loads, when there is adequate inductive energy to achieve ZVS (Fig 2(c)). At light loads, the auxiliary circuit provides the extra energy required to complete the ZVS transient.

2) DAB: Similar to ARCP, leakage inductance resonates with snubber capacitors to achieve ZVS. By resonating leakage inductance and snubber capacitors, ZVS is achieved once there is enough energy circulating in transformer leakage inductance.

III. LOSS EVALUATION
The design of a distribution level 20 kVA SST was performed for all four candidate configurations. The key parameters of switching device in each stage are listed in Table I. Three major sources of loss were evaluated: conduction loss, switching loss, and transformer loss. This study did not address power losses in the gate driver, controller, and other accessory circuits.

A. Conduction Loss
1) PWM Voltage Source Converter: Each power semiconductor device in the current conduction path has forward voltage drop, which contributes to conduction loss. The forward voltage can be modeled as

\[ v_{ce} = v_{ce0} + R_{on, t} i_f \]  \hspace{1cm} (1)

for a transistor and

\[ v_f = v_{f0} + R_{on, t} i_f \]  \hspace{1cm} (2)
for a diode.

When using SPWM, the duty ratios of transistor and diode are
\[ d_T = \frac{1}{2} \left( 1 + m \sin(\omega t) \right) \] and
\[ d_D = \frac{1}{2} \left( 1 - m \sin(\omega t) \right), \]
respectively [7]. Integrating instantaneous conduction loss \( v \cdot i \cdot d \) over one grid period, the conduction loss of transistor is

\[ P_{\text{cond},T} = \left( \frac{r_m}{2} + \frac{m \cos \phi}{3} \right) \frac{V_m^2}{4\pi} + \left( 2 + \frac{\pi}{2} \cos \phi \right) \frac{V_m I_m}{4\pi} \]  
and the conduction loss of diode is

\[ P_{\text{cond},D} = \left( \frac{r_m}{2} - \frac{m \cos \phi}{3} \right) \frac{V_m^2}{4\pi} + \left( 2 + \frac{\pi}{2} \cos \phi \right) \frac{V_m I_m}{4\pi} \]  

A high-voltage rectifier is a voltage source converter controlled by PWM with a power factor correction loop. Therefore, its conduction pattern is similar to that of a VSC inverter with a fixed load power factor at steady state. Thus, the conduction loss of high-voltage rectifier can also be calculated using (3) and (4).

2) Dual Active Bridge Converter: DAB converters transfer active power from the leading bridge to the lagging bridge. Once the amount of transferred power is determined, the phase shift angle can be calculated as

\[ \phi = \frac{\pi}{2} \left( 1 - \sqrt{1 - \frac{4N \omega L_T P}{\pi V_i V_o}} \right). \]  

Then the boundary currents between switching states (Fig. 3) are:

\[ i_0 = \frac{(\pi - 2\phi) V_o - \pi V_i}{2\omega L_1}, \]  

and

\[ i_\phi = \frac{\pi V_o - (\pi - 2\phi) V_i}{2\omega L_1}. \]  

For dc-dc DAB converters used in the SST2 and SST3, transistors are conducting when transformer instantaneous current is positive, and diodes are conducting at negative current. Finally, the conduction loss of leading bridge is

\[ P_{\text{cond},\text{lead}} = 2 \left( i_0 v_f d_1 + i_\phi v_{ce} d_2 + \frac{\pi - \phi}{\pi} \right), \]  

and conduction loss of lagging bridge is

\[ P_{\text{cond},\text{lag}} = 2 \left( i_0 v_f \left( d_1 + \frac{\pi - \phi}{\pi} \right) + i_\phi v_{ce} d_2 \right), \]  

where \( d_1 = \frac{i_o}{i_f + i_o} \) and \( d_2 = \frac{i_\phi}{i_f + i_\phi} \).

The conduction loss of ac-ac DAB converters (SST4) can be calculated in a different way. Note that there are always series-connected IGBT-diodes in the conduction path of each switching cell in the ac-dc DAB converters. The current waveform showed in Fig. 3 is triangular from 0 to \( \alpha \) and from \( \alpha \) to \( \phi \), and trapezoidal from \( \phi \) to \( \pi \). Using the symmetry of current waveform, the RMS current during one switching period is

\[ I_{\text{rms}} = \frac{1}{\sqrt{3}} \left[ 2i_0^2 + 2i_\phi^2 + \frac{\phi}{\pi} \left( i_0^2 + i_\phi^2 \right) \right]. \]  

Finally, the conduction loss of one bridge is

\[ P_{\text{cond}} = I_{\text{rms}}^2 \left( R_{\text{on,t}} + R_{\text{on,d}} \right) + I_{\text{rms}} \left( v_{ce0} + v_f0 \right). \]  

B. Switching Loss

1) Hard Switching: When hard switching is applied to the inverter and rectifier stages, the average IGBT turn-on/turn-off energy and the diode reverse recovery energy can be determined from the device datasheets. Since the number of
commutation from IGBTs to diodes is equal to the number of commutation from diodes to IGBTs, switching loss is

\[ P_{sw} = \frac{f_{sw}}{\pi} (E_{on} + E_{off} + E_{rr}) \]  

where turn-on loss \( E_{on} \), turn-off loss \( E_{off} \), and diode reverse recovery loss \( E_{rr} \) are linearly related to load current and bus voltage.

2) ARCP Soft Switching: The switching loss of ARCP consists of three parts: main switch soft switching loss, extra main switch conduction loss, and auxiliary switch conduction loss.

(i) During ZVS transient, the \( \frac{dv}{dt} \) of IGBT is limited by its snubber capacitor. IGBT turn-off energy under ZVS is \( E_{zvs} = \frac{i_{r}^{2}C}{2} \). Thus, IGBT turn-off loss is given by

\[ P_{sw,ARCP} = 2f_{sw} \frac{t_{f}^{2}}{6C_{r}} \sum_{i=1}^{K} (i_{r}^{2} + i_{d}^{2}) \]  

where \( K = \frac{t_{sw}}{t_{f}} \), turn-off current for diode switching is \( i_{d} = I_{m} \sin \omega t + I_{boost,d} \), and turn-off current for IGBT switching is

\[ i_{t} = \begin{cases} I_{m} \sin \omega t, & \text{for ARCP disabled} \quad (14a) \\ I_{m} \sin \omega t + I_{boost,t}, & \text{for ARCP enabled} \quad (14b) \end{cases} \]

A detailed explanation can be found in [6].

(ii) Beside conducting load current, the main switches must conduct extra boost current from the auxiliary switches. The extra current is used to provide the inductive energy to achieve ZVS. Using waveform symmetry, this extra conduction loss is

\[ P_{Aux1} = 2f_{sw} \frac{L_{r}}{V_{dc}} (i_{r}^{2} + i_{t}^{2}) (V_{f} + V_{cc}) \]  

(iii) Auxiliary switching turns on-and-off at zero current during ARCP transients. Therefore, the switching loss of auxiliary switches is neglected. However, the auxiliary switches do conduct a significant amount of current to realize ZVS for the main switches. For diode-to-IGBT commutation, there are three portions of current through the auxiliary switches: linear charging current, half-period resonant transient current, and linear discharging current. For IGBT-to-diode commutation, there is an auxiliary circuit conduction loss only when ARCP is enabled. Combining these two scenarios, the power loss in this portion is given by

\[ P_{Aux2} = 2f_{sw} \frac{L_{r}}{V_{dc}} \left( i_{r}^{2} + \pi \sqrt{2L_{r}C_{r}} \right) (V_{cc} + V_{f}) + \]  

\[ 2f_{sw} \sum_{i=1}^{N} \frac{t_{i}^{2}}{2} \left( \frac{L_{r}}{V_{dc}} i_{t}^{2} + \pi \sqrt{2L_{r}C_{r}} \right) (V_{cc} + V_{f}) \]  

where \( N \) is the number of switching transients when ARCP is enabled for transistor-to-diode switching.

3) DAB Soft Switching: When designed properly, dc-dc DAB converters allow ZVS over a wide operating range. Switching devices are turned on and off with ZVS. ZVS turn-on energy is close to zero, and turn-off energy can be calculated as

\[ P_{DAB,dc} = 4f_{sw} \frac{t_{f}^{2}}{6C_{r}} \left( i_{r}^{2} + i_{d}^{2} \right) \]  

where \( t_{f} \) is the fall time of IGBT, \( C_{r} \) is resonant capacitance, and \( f_{sw} \) is switching frequency.

The switching loss of an ac-ac DAB converter is slightly different from that of its dc-dc counterpart. Both \( i_{0} \) and \( i_{\phi} \) vary sinusoidally. ZVS is valid when instantaneous current is high. Therefore, switching energy can be calculated as

\[ E_{sw,soft} = \frac{t_{f}^{2}}{6C_{r}} (i_{r}^{2} + i_{d}^{2}) \]  

When ZVS is not valid around zero-crossing points, hard switching energy is

\[ E_{sw,hard} = E_{on} + E_{off} + \frac{1}{2} C_{r} V^{2} \]  

where the turn-on and turn-off energy of switching devices can be found in the manufacturers datasheets and the last term of (19) represents the energy lost in resonant capacitors. The switching loss of ac-dc DAB converter is

\[ P_{DAB,ac-dc} = f_{sw} \frac{t_{f}^{2}}{N} \left( N_{soft} E_{sw,soft} + N_{hard} E_{sw,hard} \right) \]  

where \( N \) is the number of switching commutation events is a single 60-Hz cycle, \( N_{soft} \) and \( N_{hard} \) are the numbers of soft-switching and hard-switching events, respectively, in one mains cycle.

C. Transformer Copper Loss

The transformer in a DAB converter operates at a frequency range of several kilo-hertz where the skin depth of wire is close to the wire diameter. Therefore, the high-frequency effect on winding resistance can be significant. The ac winding resistance of a high-frequency transformer is calculated using the orthogonality between skin effect and proximity effect [8]. Ac resistance is the product of dc resistance and a factor representing skin and proximity effects:

\[ k = \frac{\sinh(\xi(\eta)) + \sin(\xi(\eta))}{\cosh(\xi(\eta)) - \cos(\xi(\eta))} \eta^{2} (2m - 1) \frac{\sinh(\xi(\eta)) - \sin(\xi(\eta))}{\cosh(\xi(\eta)) + \cos(\xi(\eta))} \]
where $\xi(\eta) = \frac{\sqrt{2} \eta}{\sqrt{\pi} d(\eta)}$ and $\delta(\eta) = \frac{1}{\sqrt{\pi f \mu_0 \rho}}$. The dc component of winding resistance is $R_{dc} = \frac{\omega N L}{A}$ where $N$ is the total number of turns and $A$ is the copper area of the wire. Copper loss is calculated using winding ac resistance and RMS current:

$$P_{cu} = I_{rms, pri}^2 R_{ac, pri} + I_{rms, sec}^2 R_{ac, sec}. \quad (22)$$

D. Transformer Core Loss

According to [9], peak flux density is

$$B_{acc} = \frac{V_{rms} \times 10^4}{4.44N f A_e}, \quad (23)$$

where $A_e$ is the core area of the magnetic core. Core loss depends on magnetic flux, operating frequency, the core weight, and the voltage waveform. For simplicity, it is given by

$$P_{core} = k f^m B_{acc}^n \quad (24)$$

where parameters $k$, $m$, and $n$ for a given core material can be found in [9] or the manufacturer’s datasheets.

IV. RESULTS

This study evaluated seven cases: SST1, SST2 and SST3 with hard switching and with soft switching, respectively, and SST4 with soft switching. Fig. 4(a) and Fig. 4(b) show the loss breakdown for these seven cases. Table II and Table III show loss and efficiency at full load and 33 % load, respectively.

Fig. 5 shows the efficiency of SST2 with hard switching under different load apparent power and load power factor. In Fig. 5, SST’s efficiency drops drastically at light load conditions.

The efficiency of all four SST topologies is lower than that of conventional magnetic transformer due to the addition of power electronic converters. Among all four configurations, SST1 is the most efficient topology; however, it lacks the size advantage of a high-frequency transformer. Efficiency decreases as the power converters become more complex. The efficiency of SST3 is slightly better than that of SST2 due to the reduction of switching frequency by using a multilevel front-end rectifier. SST4 has higher efficiency because it benefits from less energy circulation and less number of power conversion stages; however, it lacks a low voltage dc port and reactive power control.

Comparing hard switching and soft switching, ARCP increases efficiency at the expense of increasing circuit complexity even further. It is costly to implement ARCP at the 7.2 kV high voltage side. Furthermore, the effect of loss reduction becomes less significant at light loads for fixed timing ARCP. DAB converters achieve soft switching without introducing extra switching devices. However, the soft switching range depends on the converter parameters. Under light load conditions, the soft-switching range of DAB converters (both dc-dc and ac-ac) is narrower, resulting in more switching loss.
### TABLE II

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V. DISCUSSION AND CONCLUSION

Although the power efficiency of the current generation of SSTs is not competitive with conventional passive transformers, SST is still attractive by increasing the overall efficiency of the distribution system. An SST (except SST4) can increase power factor by reactive power control. In this way the loss caused by reactive current is reduced, which can fully or partially compensate the increased loss by SST itself.

The power efficiency of all three stages in an SST needs improvement.

1) For the low voltage inverter, it might be advantageous to replace IGBTs with high voltage MOSFETs, such as those with SuperMESH technology.

2) For the high voltage rectifier, the key issue is availability of new generation of power semiconductor device.

3) For the DAB stage, it is necessary to develop a control method to increase efficiency at low power conditions. It is also interesting to find a circuit parameter optimization method.

It is necessary to develop a system-level loss estimation framework to analyze the effect of SSTs’ power flow control and power factor correction capability on the overall efficiency of a distribution grid.

ACKNOWLEDGMENT

This work was supported by ERC Program of the National Science Foundation under Award Number EEC-08212121.

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